

Ronald O'neal

CONVEX Maintenance Documentation
Overview
(C201, C202, C210, C220)
Document No. 081-000003-201

First Edition, Rev. 1
February 1989

CONVEX Computer Corporation
Richardson, Texas USA

CONVEX Maintenance Documentation Overview
(C201, C202, C210, C220)
Order No. DHW-100
First Edition, Rev. 1

© 1988 CONVEX Computer Corporation
All rights reserved.

This document is copyrighted. All rights are reserved. This document may not, in whole or part, be copied, duplicated, reproduced, translated, electronically stored, or reduced to machine readable form without prior written consent from CONVEX Computer Corporation (CONVEX).

Although the material contained herein has been carefully reviewed, CONVEX does not warrant it to be free of errors or omissions. CONVEX reserves the right to make corrections, updates, revisions, or changes to the information contained herein. CONVEX does not warrant the material described herein to be free of patent infringement.

UNLESS PROVIDED OTHERWISE IN WRITING WITH CONVEX COMPUTER CORPORATION (CONVEX), THE EQUIPMENT DESCRIBED HEREIN IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. SOME STATES DO NOT ALLOW THE EXCLUSION OF IMPLIED WARRANTIES. THE ABOVE EXCLUSION MAY NOT BE APPLICABLE TO ALL PURCHASERS BECAUSE WARRANTY RIGHTS CAN VARY FROM STATE TO STATE. IN NO EVENT WILL CONVEX BE LIABLE TO ANYONE FOR SPECIAL, COLLATERAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING ANY LOST PROFITS OR LOST SAVINGS, ARISING OUT OF THE USE OR INABILITY TO USE THIS EQUIPMENT. CONVEX WILL NOT BE LIABLE EVEN IF IT HAS BEEN NOTIFIED OF THE POSSIBILITY OF SUCH DAMAGE BY THE PURCHASER OR ANY THIRD PARTY.

CONVEX and the CONVEX logo ("C") are registered trademarks of CONVEX Computer Corporation
C201, C202, C210, C220, and C200 Series are trademarks of CONVEX Computer Corporation

Printed in the United States of America

Revision Sheet

CONVEX Maintenance Documentation Overview (C201, C202, C210, C220)

Edition	Document No.	Date	Description
First	081-000003-200	September 1988	Describes the five manuals comprising the <i>CONVEX Maintenance Documentation</i> kit. Provides a master table of contents, index, and glossary to all manuals.
First, Rev. 1	081-000003-201	February 1989	Minor corrections made to Volumes I-IV and VI; corrections and major additions made to Volume V.

THIS PAGE INTENTIONALLY LEFT BLANK

Table of Contents

1 Introduction	
1.1 Overview	I.1-1
1.2 Scope	I.1-1
1.3 Documents Included	I.1-1
1.4 Dependencies	I.1-2
1.5 Master Table of Contents	I.1-2
1.6 Master Index	I.1-2
1.7 Master Glossary	I.1-2
1.8 Associated Documentation	I.1-3
1.8.1 Ordering Documentation	I.1-3
1.8.2 Technical Assistance	I.1-4
2 Master Table of Contents	
2.1 Overview	I.2-1
3 Master Index	
3.1 Overview	I.3-1
4 Glossary	
4.1 Overview	I.4-1
4.2 Terms	I.4-1

THIS PAGE INTENTIONALLY LEFT BLANK

Chapter 1

Introduction

1.1 Overview

CONVEX Maintenance Documentation (C201, C202, C210, C220) contains five separate volumes of maintenance materials plus this overview manual. This manual introduces the structure of the *CONVEX Maintenance Documentation (C201, C202, C210, C220)*. It also includes a master table of contents, a master index, and a master glossary to all six volumes.

The *CONVEX Maintenance Documentation (C201, C202, C210, C220)* is a reference tool for CONVEX personnel who maintain CONVEX equipment and CONVEX customers who do their own maintenance.

1.2 Scope

The *CONVEX Maintenance Documentation* applies to the CONVEX C201, C202, C210, and C220 supercomputers.

1.3 Documents Included

This documentation kit includes the following six maintenance manuals:

- Volume I, *CONVEX Maintenance Documentation Overview (C201, C202, C210, C220)*—Use this manual to obtain a general overview of the documentation as well as find the master table of contents, master index, and master glossary to all documentation.
- Volume II, *CONVEX Theory of Operation (C201, C202, C210, C220)*—This document contains a broad system-level introduction and theory to the level necessary to support maintenance.
- Volume III, *CONVEX Installation Guide (C201, C202, C210, C220)*—This volume provides procedures for installing a system at a new site and for upgrading a system at an existing site.
- Volume IV, *CONVEX General Maintenance Guide (C201, C202, C210, C220)*—This document provides a preventive maintenance schedule and procedures for maintaining a system on a monthly and quarterly basis.
- Volume V, *CONVEX Troubleshooting Guide (C201, C202, C210, C220)*—This document provides indicator and error message information, troubleshooting procedures and flow charts, and a troubleshooting philosophy and methodology discussion.
- Volume VI, *CONVEX Removal/Replacement and IPB Guide (C201, C202, C210, C220)*—This guide provides the Field Engineer (FE) with the information required to remove, order, and install components in the computer.

1.4 Dependencies

All volumes in this kit are designed to be used together to eliminate excessive repetition of technical data between manuals and to simplify the revision process. The master table of contents, master index, and master glossary are comprehensive reference tools that make using the kit easier.

1.5 Master Table of Contents

A master table of contents, in Chapter 2, contains an exact copy of the table of contents of each volume.

1.6 Master Index

The master index, in Chapter 3, makes finding a particular subject easier across all volumes. The index contains symbol and numeric sections as well as the usual alphabetical section. Alphabetization is in the following order:

1. symbols
2. numerals
3. letters from A to Z

Each section is preceded by a boldfaced title. Preceding each page number (which is the chapter number followed by a dash then the page number of that chapter) is a Roman numeral that indicates the volume referenced. A period is placed between the volume number and the chapter-page number. The following is an example index entry:

System Exerciser, *sysex* III.8-2, IV.3-5

The above entry indicates that references to the system exerciser program appear in volume III (*CONVEX Installation Guide (C201, C202, C210, C220)*) on page 2 of Chapter 8, and in volume IV (*CONVEX General Maintenance Guide (C201, C202, C210, C220)*) on page 5 of Chapter 3.

See cross-references guide the reader to preferred spellings and entry wording. *See also* cross-references point the way to related subjects.

1.7 Master Glossary

The master glossary, in Chapter 4, is a list of CONVEX-preferred technical nomenclature and terminology, including standard abbreviations.

1.8 Associated Documentation

The following is a partial list of other manuals or books that may provide more detailed information on the topics presented in this manual:

- *C190, C210, C220 System Diagnostics, Release Notice*
- *CONVEX Architecture Reference*, Product No. DHW-005
- *CONVEX Computer Site Preparation Guide (C200 Series)*, Order No. DHW-009
- *CONVEX Diagnostic Database (C190, C210, C220), Release Notice*
- *CONVEX Diagnostic Documentation (C200 Series)*, Product No. DHW-080
- *CONVEX HIA User's Guide*, Product No. DHW-035
- *CONVEX Processor Operation Guide (C100 Series, C200 Series)*, Order No. DHW-015
- *CONVEX Removable Disk System Operation Guide*, Order No. DHW-043
- *CONVEX System Manager's Guide*, Product No. DSW-004
- *CONVEX UNIX, Release Notice*
- *CONVEX VIOP/VBCU Service Guide*, Product No. DHW-051
- *FUJITSU M2951A/AF Mini Disk Drive, Customer Engineering Manual*
- *Installation Procedure, CONVEX UNIX and Utilities*
- *Printronic P6000 Maintenance Manual*, Document No. 900-000328-001
- *SPU UNIX, Release Notice*
- *STC 1960 Series Tape Drive*, Document No. 900-000253-001
- *STC 2920 Tape Subsystem Maintenance Manual*, Document No. 900-000252-001
- *VIPER Product Manual, SCSI Models 2060S and 2150S*, Document No. 900-000321-001

1.8.1 Ordering Documentation

To obtain the most current version of this or any other CONVEX document, use the order number. If the product number is not known, order by the exact title. In some situations the most current version is not desired. To receive a specific version of a manual, use the CONVEX document, or part, number, which can be obtained by contacting the local CONVEX office or by calling the Technical Assistance Center.

The product number for this manual is DHW-100.
The document number for this manual is 081-000003-201.

CONVEX documents can be ordered by mail by sending a request to:

CONVEX Computer Corporation
Customer Service
PO Box 833851
Richardson TX 75083-3851 USA

1.8.2 Technical Assistance

Hardware and software support can be obtained through the CONVEX Technical Assistance Center (TAC). The TAC can be reached in Texas by calling (214) 952-0379, or by calling 1(800) 952-0379 from other locations in the continental United States. Customers outside the United States should contact their local CONVEX office.

Electronic Mail

The Hardware Documentation Group has an email address for documentation comments. Use this service to give us a quick response mechanism if you have special documentation questions that you would like addressed immediately. If you have a technical question, you should still contact the Technical Assistance Center, as described previously. To use email response service, just send mail addressed to:

`cnvxhwdoc@convex.COM`

We will read your comments and give you a personal reply.

What to Include in an Email Message

When you use the electronic mail service, please provide the following information:

- The reader's name and company name
- A return email address in INTERNET notation or UUCP (bang) notation
- The manual that is being critiqued
- The chapter and page number in question
- The comment

Reader's Forum

If you wish to mail your comments to us, please use the form at the end of this manual and list the document page number with your questions and comments. Thank you.

Acknowledgments

I would like to thank the following people for their contributions to the volumes of this document kit:

- **Technical contributors:** Rich Adkisson, Tony Brewer, Art Clark, Mary Cooley, Brad Culter, Gary Gostin, Carl Jackson, Jeff Jones, Tony Jones, Art Kimmel, Brian Konigsburg, Kevin Lowderman, Alan Peterson, Marc Quattromani, John Rachels, and Craig Reed
- **Review team members:** Art Clark, Don Davis, Ron Engelking, Steve Fieler, Art Kimmel, and Rick Miller
- **Hardware Documentation staff:** Larry Bonura, Art Fischman, and Jimmie Holman
- **Contributing writers:** Bruce Evans, Barbara Morris, and Randy Stiles

Without the efforts of all the aforementioned, this document would not have been possible.

Leigh Ellert, Lead Writer
CONVEX Hardware Documentation

THIS PAGE INTENTIONALLY LEFT BLANK

Chapter 2

Master Table of Contents

2.1 Overview

This chapter contains the master table of contents, which gives a comprehensive outline of the six volumes in this kit.

THIS PAGE INTENTIONALLY LEFT BLANK

Master Table of Contents

Volume I CONVEX Maintenance Documentation Overview

1 Introduction

1.1 Overview	I.1-1
1.2 Scope	I.1-1
1.3 Documents Included	I.1-1
1.4 Dependencies	I.1-2
1.5 Master Table of Contents	I.1-2
1.6 Master Index	I.1-2
1.7 Master Glossary	I.1-2

2 Master Table of Contents

2.1 Overview	I.2-1
--------------------	-------

3 Master Index

3.1 Overview	I.3-1
--------------------	-------

4 Glossary

4.1 Overview	I.4-1
4.2 Terms	I.4-1

Volume II Theory of Operation

1 Introduction

1.1 Overview	II.1-1
1.1.1 Data Representations	II.1-2
1.1.2 Register Sets	II.1-2
1.1.3 Memory Management	II.1-2
1.1.4 Multiprocessor Management	II.1-3
1.1.5 Exceptions and Interrupts	II.1-4
1.2 System Descriptions	II.1-4
1.2.1 CONVEX Cabinets	II.1-5
1.2.1.1 Processor Cabinets	II.1-5
1.2.1.2 Expansion Cabinets	II.1-7
1.2.2 C200 Series System Power Requirements	II.1-8
1.3 System Architecture	II.1-8
1.4 Address/Scalar Processor Subsystem	II.1-11
1.4.1 Scalar Processor	II.1-11
1.4.2 Instruction Processor	II.1-12
1.4.3 Memory Interface	II.1-14
1.5 Vector Processor Subsystem	II.1-16
1.5.1 Memory and Scalar Processor Interface	II.1-18
1.5.2 Instruction Dispatch Control	II.1-19
1.5.3 Function Units	II.1-19
1.5.4 State Save and Restore Data	II.1-19
1.6 Memory Subsystem	II.1-19
1.7 I/O Subsystem	II.1-21
1.7.1 PBUS Interface Adapter (PIA)	II.1-21
1.7.1.1 PBUS Description	II.1-22
1.7.1.2 EBUS Description	II.1-22
1.7.2 Channel Control Unit (CCU)	II.1-23
1.7.2.1 I/O Processors	II.1-24
1.7.3 Service Processor Unit 2 (SP2)	II.1-25
1.7.3.1 SP2 Hardware	II.1-26
1.7.3.2 SP2 Indicators	II.1-27
1.7.3.3 SP2 EBUS Interface	II.1-28
1.7.3.4 System Clock Control	II.1-28
1.7.3.5 Main Memory Refresh Control	II.1-28
1.7.3.6 Diagnostic Interface	II.1-28
1.7.3.7 SP2 Peripherals	II.1-29
1.7.3.8 System Console	II.1-29
1.7.3.9 SPU Disk	II.1-30
1.7.3.10 SPU Tape Drive	II.1-30
1.7.3.11 SP2 Software	II.1-30
1.7.3.12 Operating Systems	II.1-30
1.7.3.13 Diagnostics	II.1-31
1.7.3.14 Utilities	II.1-31
1.8 Utility Subsystem	II.1-31
1.8.1 CPU Utility Unit (CPX)	II.1-31
1.8.2 System Control Monitor (SCM)	II.1-33
1.9 Processor Operation Environment	II.1-35
1.9.1 Power Up/Power Down	II.1-35
1.9.2 Soft Front Panel (Firmware)	II.1-36

1.9.3	SPU UNIX Operating System	II.1-36
1.9.4	CONVEX UNIX Operating System	II.1-36
1.9.4.1	Basic Booting Procedures	II.1-37
1.9.4.2	Power-Up Procedures	II.1-37
1.9.4.3	Bootting From Power-Up To CONVEX UNIX Multi-User Mode	II.1-40
1.9.4.4	Bootting in Diagnostic Mode	II.1-41
1.9.4.5	System Generation Overview	II.1-41
1.9.4.6	Essential System Files	II.1-43
2	C200 Series Architecture Overview	
2.1	Overview	II.2-1
2.1.1	What Makes a C2 a C200 Series Machine?	II.2-1
2.2	Extended Opcodes	II.2-2
2.3	New Vector Operations	II.2-2
2.4	Intrinsics	II.2-3
2.5	Virtual Memory Management	II.2-4
2.5.1	Shared and Unshared Memory	II.2-4
2.5.2	Thread-Level Page Table Entry (PTET)	II.2-5
2.5.3	Cache Consistency and Remote Invalidates	II.2-5
2.5.4	Unen cacheable Pages	II.2-6
2.5.5	C200 Series PTE Format	II.2-6
2.6	Communication Registers	II.2-7
2.6.1	Communication Register Addressing	II.2-7
2.6.2	Hardware Communication Registers	II.2-12
2.6.2.1	Hardware Reserved Communication Registers	II.2-13
2.6.2.2	Fork Event Communication Registers	II.2-14
2.6.2.3	Segment Descriptor Registers	II.2-15
2.6.2.4	Trap Instruction Registers	II.2-15
2.6.2.5	Thread Allocation Mask and Count	II.2-15
2.6.2.6	CPU Execution Clock Registers	II.2-16
2.6.3	Primitive Communication Register Operations	II.2-16
2.6.4	Communication Register Modified Bits and the <i>stcmr/ldcmr</i> Instructions	II.2-17
2.6.5	Memory Structures Locked with Communication Registers	II.2-18
2.7	Memory Duals of Communication Register Operations	II.2-19
2.8	Multiprocessing (Forking/ASAP)	II.2-20
2.8.1	Details of Forking Instructions	II.2-23
2.8.1.1	<i>pfork</i> <effa>,Ak	II.2-25
2.8.1.2	<i>spawn</i> <effa>,Ak	II.2-26
2.8.1.3	<i>cfork</i>	II.2-26
2.8.1.4	<i>wfork</i>	II.2-26
2.8.1.5	<i>join</i>	II.2-26
2.8.1.6	<i>idle Sk</i>	II.2-27
2.8.1.7	Microcode Idle Loop	II.2-27
2.8.2	Parallelized Loop Example	II.2-29
2.9	Page 0/Exceptions/Traps	II.2-30
2.9.1	Page 0	II.2-30
2.9.2	New PSW Bits and Traps	II.2-33
2.9.2.1	New Arithmetic Exceptions	II.2-34
2.9.2.2	New PTE Violations	II.2-34
2.9.2.3	Invalid Communication Address Exception	II.2-35
2.9.2.4	Thread Concurrency and Initialization Traps	II.2-35
2.9.2.5	Deadlocks	II.2-36
2.9.2.6	Trap and Process Breakpoint	II.2-38

2.9.2.7 C200 Series Processor Trap Mechanism	II.2-40
2.10 Interrupts	II.2-41
2.10.1 Interrupt Channels	II.2-41
2.10.2 Interrupt Processing	II.2-41
2.10.2.1 Interrupt Control Register (ICR)	II.2-42
2.10.2.2 Target CPU (TCPU) Register	II.2-43
2.10.2.3 C200 Series Interrupt Control System	II.2-43
2.10.2.4 Interrupt Context Blocks	II.2-45
2.10.2.5 Virtual Memory Mapping Restrictions	II.2-46
2.10.3 Idle CPU Interrupt Processing	II.2-46
2.10.4 Active CPU Interrupt Processing	II.2-47
2.10.4.1 Active CPU Base-Level Processing	II.2-47
2.10.4.2 Active CPU Interrupt Level Processing	II.2-48
2.10.5 Returning from a Base-Level Interrupt	II.2-48
2.10.6 General Interrupt Processing Information	II.2-48
2.11 Timers	II.2-49
2.11.1 C200 Series Interval Timer	II.2-49
2.11.1.1 Interval Timer Status Register	II.2-50
2.11.1.2 Next Interval Timer Count	II.2-50
2.11.1.3 Interval Timer Counter	II.2-51
2.11.1.4 Interval Timer Interrupt Number	II.2-51
2.11.2 Time of Century Clock (TOC)	II.2-51
2.11.3 CPU Execution Timer	II.2-52
2.11.4 Thread Timer	II.2-53
2.11.5 C200 Series CTR and TTR Manipulation	II.2-53

3 Scalar Subsystem

3.1 Overview	II.3-1
3.1.1 Register File (ASP)	II.3-2
3.1.2 Processor Status Word (ASP)	II.3-2
3.1.3 BBUS Control (SFU)	II.3-2
3.1.4 Scratch RAM (ASP)	II.3-3
3.1.5 Arithmetic and Logic Unit (ASP)	II.3-4
3.1.6 FAD Fast Adder (IPP)	II.3-4
3.1.7 SMUL Multiplication (SFU)	II.3-4
3.1.8 DIVX Divide and Square Root (SFU)	II.3-5
3.1.9 SALU Conversions and Floating Point Subtraction (SFU)	II.3-5
3.2 Instruction Processor	II.3-5
3.2.1 Instruction Cache (IPP)	II.3-6
3.2.2 Instruction Cache Operations	II.3-6
3.2.2.1 Instruction Dispatch	II.3-7
3.2.2.2 Branches and Jumps	II.3-7
3.2.2.3 Traps and Interrupts	II.3-9
3.2.2.4 Instruction Lookahead	II.3-10
3.2.2.5 Writing the Icache	II.3-10
3.2.3 Icache Valid A and Valid B (IPP)	II.3-11
3.2.4 Lookahead Cache (IPP)	II.3-11
3.2.4.1 Traps and Interrupts	II.3-12
3.2.4.2 Faults	II.3-12
3.2.5 Lookahead Valid A and Valid B (IPP)	II.3-13
3.2.6 Pre-Crack (IPP)	II.3-14
3.2.7 Memory Data Register (IPP)	II.3-14
3.2.8 Write Address Register (IPP)	II.3-15

3.2.9	Jump Address Register (IPP)	II.3-15
3.2.10	Branch Address Register (IPP)	II.3-16
3.2.11	Next Program Counter (ASP)	II.3-16
3.2.12	Lookaside Register (IPP)	II.3-16
3.2.13	Align (IPP)	II.3-16
3.2.14	Post-Crack and Dispatch Register(IPP)	II.3-17
3.2.15	Hazards	II.3-17
3.2.16	Context Bits	II.3-17
3.3	Memory Interface	II.3-18
3.3.1	Data Flow Gate Arrays (ASP)	II.3-20
3.3.2	Data Cache (ASP, DCU, SFU)	II.3-20
3.3.2.1	Dcache Data (ASP)	II.3-21
3.3.2.2	Dcache Tags	II.3-21
3.3.2.3	Validity Tags	II.3-21
3.3.2.4	Update Tags	II.3-21
3.3.2.5	Dcache Operations (ASP, DCU, SFU)	II.3-22
3.3.2.6	Byte Validity (DCU)	II.3-23
3.3.2.7	Dcache Control (DCU)	II.3-24
3.3.3	Logical-to-Physical Address Translation (SFU, DCU)	II.3-24
3.3.3.1	Swappers	II.3-24
3.3.3.2	Alpha Addressing	II.3-25
3.3.3.3	Logical Address Registers (DCU)	II.3-26
3.3.3.4	Vector Address Generator (SFU)	II.3-26
3.3.4	Memory Control (DCU)	II.3-27
3.3.4.1	Memory	II.3-28
3.3.4.2	Look-Aside-Buffer (DCU, SFU)	II.3-28
3.3.4.3	Memory Return Control (SFU)	II.3-28
3.3.4.4	Store Data Queue (ASP)	II.3-29
3.3.5	System Faults	II.3-29
3.3.5.1	Saving Fault State	II.3-30
4	Vector Subsystem	
4.1	Overview	II.4-1
4.2	Vector Processor Interfaces	II.4-3
4.3	Vector Processor	II.4-3
4.3.1	Vector Register Files	II.4-6
4.3.1.1	Vector Edit Logic	II.4-9
4.3.2	Memory and Scalar Processor Interface	II.4-9
4.3.2.1	Load and Store Function Pipe Micro Control	II.4-10
4.3.2.2	Load and Store Function Pipe Write Control	II.4-11
4.3.2.3	Input Staging	II.4-12
4.3.2.4	Output Staging	II.4-13
4.3.2.5	Vector Length Register	II.4-14
4.3.2.6	Processor Status Word Register	II.4-15
4.3.2.7	Faults	II.4-15
4.3.2.8	Instruction	II.4-16
4.3.3	Function Units	II.4-16
4.3.3.1	ALU Pipeline	II.4-17
4.3.3.2	ALU Function Pipe Unit Control	II.4-18
4.3.3.3	ALU Function Pipe Micro Control	II.4-18
4.3.3.4	ALU Function Pipe Write Control	II.4-19
4.3.3.5	MFU Pipeline	II.4-19
4.3.3.6	Multiply Function Pipe Unit Control	II.4-20

4.3.3.7 Multiply Function Pipe Micro Control	II.4-20
4.3.3.8 Multiply Function Pipe Write Control	II.4-21
4.3.3.9 Divide Function Unit Control	II.4-21
4.3.4 Vector Merge Register	II.4-22
4.3.4.1 VM Bit Output Staging Controller	II.4-22
4.3.4.2 State Save and Restore Data	II.4-23
4.3.5 Clock Generation Logic	II.4-23

5 Memory Subsystem

5.1 Overview	II.5-1
5.1.1 Organization	II.5-2
5.1.2 Memory Control Module	II.5-6
5.1.2.1 MCM Processor Port I/O	II.5-8
5.1.2.2 MCM Control I/O	II.5-8
5.1.2.3 Memory Cycle Types	II.5-9
5.1.3 Memory Array Module	II.5-10
5.1.4 Memory Bank	II.5-10
5.1.5 Arbitration Controller	II.5-12
5.1.6 Address and Data Crossbar	II.5-14
5.1.7 Read Multiplexer	II.5-17
5.1.8 Clock Generator	II.5-17
5.1.9 Scan Control	II.5-17
5.1.10 Win Queue	II.5-18
5.1.11 Miscellaneous Logic	II.5-19
5.1.12 Capacity	II.5-20
5.1.13 Memory Interleaving	II.5-21
5.1.14 Bandwidth	II.5-22
5.1.15 Memory Contentions	II.5-23
5.1.16 Memory Addressing	II.5-23
5.1.17 Memory Loading	II.5-24

6 Input/Output Subsystem

6.1 Overview	II.6-1
6.2 PIA—PBUS Interface Adapter	II.6-2
6.2.1 PBUS Interface Capacity	II.6-2
6.2.2 PBUS Interface	II.6-2
6.2.2.1 PBUS Arbitration	II.6-3
6.2.2.2 PBUS Arbiter	II.6-3
6.2.3 EBUS Description	II.6-3
6.2.3.1 Memory Data Path	II.6-3
6.2.3.2 Memory Control Path	II.6-4
6.2.4 EBUS Interface	II.6-4
6.2.4.1 EBUS Arbitration	II.6-4
6.2.4.2 Physical Address Mapping	II.6-4
6.2.4.3 EBUS Arbiter	II.6-5
6.2.4.4 EARB/PBUS Arbiter Interface	II.6-5
6.2.4.5 EARB/Return Queue Interface	II.6-6
6.2.4.6 EARB/SP2 Interface	II.6-6
6.2.4.7 EARB Internals	II.6-6
6.2.4.8 Return Queue	II.6-7
6.2.5 Interrupt Interface	II.6-9
6.2.5.1 Interrupt Arbiter	II.6-9
6.2.5.2 Interrupt Arbitration	II.6-9

6.2.5.3	Interrupt Level Translation	II.6-9
6.2.5.4	Interrupt State machine	II.6-9
6.2.6	PIA Data Flow	II.6-9
6.2.6.1	PBUS Header Transfers	II.6-10
6.2.6.2	PBUS Write Transfers	II.6-10
6.2.6.3	PBUS Read Transfers	II.6-12
6.2.6.4	PBUS TAM Transfers	II.6-13
6.2.6.5	PBUS Memory Base Pointer Read Transfer	II.6-13
6.2.6.6	SP2 Write Transfers	II.6-13
6.2.6.7	SP2 Read/TAM Transfers	II.6-14
6.2.7	Error Handling	II.6-14
6.2.7.1	Hard Error Conditions	II.6-14
6.2.7.2	Soft Error Conditions	II.6-15
6.2.8	Clock Generation Logic	II.6-16
6.3	PBUS—Peripheral Bus	II.6-20
6.3.1	PBUS Data Transfer Operations	II.6-21
6.3.1.1	Bus Arbitration	II.6-21
6.3.1.2	Bus Acquisition	II.6-21
6.3.1.3	Bus Release	II.6-21
6.3.1.4	Bus Lock	II.6-22
6.3.1.5	Arbitration Considerations	II.6-22
6.3.2	PBUS Transactions	II.6-22
6.3.2.1	Header Longword	II.6-22
6.3.2.2	Transaction Types	II.6-23
6.3.2.3	Alignment and Partial Transfers	II.6-24
6.3.2.4	Data Transfer	II.6-25
6.3.2.5	Errors	II.6-25
6.3.3	PBUS Interrupts	II.6-25
6.3.3.1	Interrupt Vector Assignment	II.6-26
6.3.3.2	Interrupt Signal Timing	II.6-26
6.3.3.3	Interrupt Bus Cycle	II.6-26
6.3.4	PBUS Signal Line Characteristics	II.6-27
6.4	CCU—Channel Control Unit	II.6-27
6.4.1	VME Subsystem Data Path	II.6-28
6.4.2	VIOP—VME I/O Processor	II.6-29
6.4.3	VBCU—VME Bus Control Unit	II.6-31
6.4.4	VMEbus Arbitration	II.6-32
6.4.5	MIOP—Multibus I/O Processor	II.6-32

7 Utility Subsystem

7.1	Overview	II.7-1
7.2	CPX—CPU Utility Unit	II.7-3
7.2.1	I/O Access Ports	II.7-3
7.2.2	Arbitration and Crossbar Gate Arrays	II.7-4
7.2.3	Referenced and Modified Bits	II.7-6
7.2.4	Physical Configuration Map	II.7-8
7.2.5	Interval Timer and Time of Century Counter	II.7-9
7.2.5.1	Interval Timer	II.7-9
7.2.5.2	Time of Century Counter	II.7-11
7.2.6	Communication Registers	II.7-12
7.2.7	CPU Interrupt Arbitrator	II.7-13
7.2.8	Miscellaneous Logic and Error Detection	II.7-14
7.2.9	Board Level Control	II.7-14

7.3 SCM—System Control Monitor II.7-15

7.3.1 SP2 and SCM Communications II.7-15

7.3.2 SCM Reads and Writes II.7-17

7.3.3 Interrupts II.7-17

7.3.3.1 Interrupt Handling II.7-18

7.3.4 Pre-power Up Sequence II.7-18

7.3.5 Power-Up Sequence II.7-19

7.3.6 Normal Operation II.7-21

7.3.7 Environment Monitoring II.7-21

7.3.8 Power Failure Sequencing II.7-22

7.3.9 SCM Hardware II.7-23

7.3.9.1 Power Supplies II.7-23

7.3.9.2 Front Panel Indicators II.7-24

Appendixes

A Essential System Files

A.1 Overview II.A-1

A.2 List of Files Sorted by Name II.A-1

B C200 Vector Instruction Operation

B.1 Vector Instruction Overview II.B-1

B.1.1 Load Vector Register II.B-1

B.1.2 Store Vector Register II.B-2

B.1.3 Load Vector Register/Vector Index II.B-2

B.1.4 Store using Vector Index II.B-3

B.1.5 Store Scalar Extended Under Mask II.B-3

B.1.6 Move Scalar to Vector Element II.B-3

B.1.7 Move Vector Element/Scalar II.B-4

B.1.8 Load VL II.B-4

B.1.9 Load VM II.B-4

B.1.10 Store VM II.B-5

B.1.11 ALU Pipe Vector Result Operations II.B-6

B.1.12 ALU Pipe Compare Operations II.B-7

B.1.13 ALU Pipe Reduction Operations II.B-7

B.1.14 Multiply Pipe Multiply/Divide/Square Root Operations II.B-8

B.1.15 Multiply Pipe Vector Edit Operations II.B-9

B.1.16 Multiply Pipe Reduction Operations II.B-9

B.2 Memory Fault Operation II.B-10

C Reporting Problems

C.1 Overview II.C-1

C.2 Information Required to Report a Problem II.C-1

List of Tables

1-1 Address/Scalar Unit Functions II.1-11

1-2 Power-Up Procedures II.1-39

1-3 Booting From Power-Up To CONVEX UNIX Multi-User II.1-41

2-1 Communication Register Address Mapping II.2-11

2-2 Trace Trap Class Codes and Qualifiers II.2-36

2-3 Deadlock Detection Instructions II.2-37

2-4 Process Deadlock Class Codes and Qualifiers II.2-38

3-1	BBUS Arbitration Control	II.3-3
3-2	FAD Control States	II.3-4
3-3	Icache Memory Allocation	II.3-6
3-4	Memory Data Layout	II.3-14
3-5	Jump Instruction Execution Times	II.3-15
3-6	Dcache Operations	II.3-22
3-7	Longword Address Bits	II.3-25
3-8	Alpha Addressing	II.3-25
3-9	Alpha8 Addressing	II.3-26
3-10	Processor-to-Memory Control Priorities	II.3-27
4-1	VRF Input Bits	II.4-9
4-2	Requests to the Output Stage Controller	II.4-13
4-3	Function Unit Gate Array Operations	II.4-17
4-4	ALU Pipeline Functions	II.4-17
4-5	Multiply Pipeline Operation Times	II.4-19
4-6	DIVX Function Throughput Times	II.4-20
4-7	DIVX Function Throughput Times	II.4-22
4-8	Vector Processor Clocks	II.4-24
5-1	Scan Control Modes	II.5-9
5-2	MCM Cycle Types	II.5-10
5-3	Memory Chip Size to MAM Population	II.5-20
5-4	MAM to MCM Configuration	II.5-20
5-5	C200 Series Interleaving and Numeric Precision	II.5-21
5-6	C200 Series Memory Subsystem Bandwidth	II.5-23
5-7	MCM Memory Addressing	II.5-24
6-1	PBUS Transaction Types	II.6-23

List of Figures

1-1	CONVEX C201, C202, C210, C220 Hardware Components	II.1-5
1-2	Processor Cabinet Backplane—C201, C202, C210, C220	II.1-7
1-3	C200 Series CPU Functional Block Diagram	II.1-9
1-4	C200 Series System Functional Block Diagram	II.1-10
1-5	CPU Scalar Processor (SP) Functional Block Diagram	II.1-12
1-6	CPU Instruction Processor (IP) Functional Block Diagram	II.1-14
1-7	CPU Memory Interface (MI) Functional Block Diagram	II.1-15
1-8	CPU Vector Processor (VP) Subsystem Functional Block Diagram	II.1-17
1-9	Memory Subsystem Functional Block Diagram	II.1-20
1-10	I/O Subsystem Functional Block Diagram	II.1-21
1-11	CCU Subsystem Functional Diagram	II.1-23
1-12	I/O Processor Subsystem Functional Diagram	II.1-25
1-13	Service Processor Unit 2 (SP2) Functional Block Diagram	II.1-27
1-14	CPU Utility Unit (CPX) Functional Block Diagram	II.1-32
1-15	System Control Monitor (SCM) Functional Block Diagram	II.1-34
2-1	C200 Series PTE Formats	II.2-7
2-2	C200 Series Communication Register CIR Division	II.2-8
2-3	C200 Series Logical-to-Physical Mapping For 1 CIR	II.2-10
2-4	C200 Series Physical Communication Address Mapping	II.2-11
2-5	C200 Series Hardware Communication Registers	II.2-13
2-6	C200 Series Hardware Reserved Communication Registers	II.2-14
2-7	C200 Series <i>ldcmr/stcmr</i> Memory Map	II.2-17
2-8	Word and Longword Resource Structure Format	II.2-19
2-9	Word Resource Structure With Two Pushed Entries	II.2-20

2-10 Symmetric Parallel Processing	II.2-22
2-11 Asymmetric Parallel Processing	II.2-23
2-12 Fork Event Registers	II.2-24
2-13 Page 0 Logical Memory Organization	II.2-31
2-14 Stack Resource Structure Accessing	II.2-33
2-15 C200 Series Processor Status Word (PSW)	II.2-33
2-16 Trap Instruction Register Partitioning	II.2-39
2-17 Interrupt Control Register (ICR)	II.2-42
2-18 Interrupt Flow—C220	II.2-44
2-19 Interrupt Context Block	II.2-45
2-20 C200 Series Interval Timer Format	II.2-50
2-21 C200 Series Interval Timer Status Register	II.2-50
2-22 C200 Series 64-Bit TOC Clock	II.2-51
2-23 C200 Series CPU Execution Timers	II.2-52
3-1 Scalar Processor Subsystem Functional Block Diagram	II.3-1
3-2 Jumps That Cause Dispatch Lockup	II.3-13
3-3 Memory Address Paths	II.3-19
4-1 Vector Processor Subsystem Functional Block Diagram	II.4-2
4-2 Vector Processor Data Pathways	II.4-4
4-3 Vector Processor Control	II.4-5
4-4 Vector Register File Gate Arrays	II.4-7
4-5 Input Staging Pipeline	II.4-8
4-6 Input Staging to the VRF	II.4-12
4-7 Output Staging Pipeline	II.4-14
5-1 Memory Subsystem Functional Block Diagram	II.5-2
5-2 Even and Odd Memory in a C200 Series System	II.5-3
5-3 Even and Odd Memory Buses in a C200 Series System	II.5-4
5-4 Flow Diagram of a Read Request to Even and Odd Memory	II.5-5
5-5 An MCM Containing 4 MAMs and 8 Banks of Memory	II.5-7
5-6 Eight-Way Interleaving of One MCM Pair	II.5-22
5-7 MCM Memory Addressing in the Memory Subsystem	II.5-24
5-8 An Eight-Bit Load	II.5-25
5-9 A 32-Bit Load	II.5-26
5-10 A 64-Bit Load	II.5-27
6-1 I/O Subsystem Functional Block Diagram	II.6-1
6-2 CONVEX C100/C200 Series PBUS Structure	II.6-21
6-3 Header Longword	II.6-23
6-4 C200 Series VME Subsystem Block Diagram	II.6-29
6-5 VIOP Functional Diagram	II.6-30
7-1 Utility Subsystem	II.7-2
7-2 CPX Functional Block Diagram	II.7-5
7-3 Interval Timer Functional Diagram	II.7-10
7-4 Time of Century Counter Functional Diagram	II.7-11
7-5 SP2 Command Sequencing	II.7-16
7-6 SCM Power-Up Flow Diagram	II.7-20
C-1 Sample <i>contact</i> Session	II.C-3

Volume III CONVEX Installation Guide

1 Introduction

1.1 Overview	III.1-1
1.2 Customer Responsibilities	III.1-1
1.2.1 Preparing the Site	III.1-1
1.2.2 Accepting the Equipment	III.1-1
1.3 Field Engineer Responsibilities	III.1-2
1.3.1 Unpacking the Equipment	III.1-2
1.3.2 Installing the Cabinets	III.1-2
1.3.3 Connecting and Testing the AC Power	III.1-2
1.3.4 Checking the System	III.1-3
1.3.5 Installing Software	III.1-3
1.3.6 Completing the Installation Report	III.1-3

2 Safety Considerations

2.1 Overview	III.2-1
2.2 Moving Equipment	III.2-1
2.3 Input Power Rating	III.2-1
2.3.1 Power Label Description	III.2-2
2.3.2 Input Power Inspection Checklist	III.2-4
2.3.3 Power Cord Caution Labels	III.2-4
2.3.4 Power Cord Voltage Labels	III.2-6
2.3.5 Circuit Breakers	III.2-7
2.4 Mechanical Safety Procedures	III.2-9
2.5 Electrical Safety Precautions	III.2-11
2.6 Electrostatic Discharge Precautions	III.2-12

3 Unpacking

3.1 Overview	III.3-1
3.2 Checking the Inventory	III.3-1
3.3 Inspecting for Damage	III.3-3
3.4 Unpacking	III.3-3
3.4.1 Tools	III.3-3
3.4.2 Cabinets	III.3-4
3.4.2.1 Removing Packaging Around the Cabinets	III.3-5
3.4.2.2 Removing the Processor from the Pallet	III.3-5
3.4.3 Accessories	III.3-8

4 New System Cabinet Installation

4.1 Overview	III.4-1
4.2 Cabling	III.4-1
4.2.1 Tools	III.4-1
4.2.2 Modem and Terminal	III.4-2
4.2.3 Channel Control Unit Cables	III.4-2
4.2.3.1 Multibus Cables	III.4-4
4.2.3.2 VMEbus Input/Output Processor Cables	III.4-5
4.2.3.3 Removable Disk System Cables	III.4-6
4.2.4 Power Sequencing Cable	III.4-6
4.3 Securing the Cabinets	III.4-6

5 System Upgrade Cabinet Installation

5.1 Overview	III.5-1
5.2 C1 to C210 or C220 Upgrade	III.5-1
5.2.1 Tools	III.5-2
5.2.2 Removing the C1	III.5-2
5.2.3 Adding a Power Controller in the Expansion Cabinet	III.5-3
5.2.4 Installing the Multibus Chassis	III.5-4
5.2.4.1 Unpacking the Multibus Chassis	III.5-6
5.2.4.2 Transferring Controller Cards	III.5-7
5.2.4.3 Cabling the Multibus	III.5-7
5.2.5 Transferring the Slide-Mounted Peripheral Devices	III.5-14
5.2.5.1 Uncabing the Peripheral Device	III.5-16
5.2.5.2 Transferring the Drive	III.5-18
5.2.6 Cabling the Disk Drives	III.5-21
5.2.6.1 Non-Daisy-Chained Controller Cables	III.5-21
5.2.6.2 Daisy-Chained Controller Cables	III.5-24
5.2.7 VMEbus Input/Output Processor Cables	III.5-26
5.2.8 Removable Disk System Cables	III.5-26
5.2.9 AC Power Power Sequencing Cables	III.5-26
5.2.10 Installing the Cabinets	III.5-27
5.3 C210 to C220 Upgrade	III.5-27

6 AC Power

6.1 Overview	III.6-1
6.1.1 Power Connections	III.6-1
6.1.2 Wiring and Voltages Checks	III.6-2
6.2 AC Power Connections	III.6-2
6.2.1 Domestic Systems	III.6-2
6.2.1.1 Delta vs. Wye AC Power Source	III.6-3
6.2.1.2 Attaching AC Power Receptacle	III.6-3
6.2.1.3 Hard-Wired Connection	III.6-6
6.2.2 International Systems	III.6-9
6.3 AC Power Check	III.6-11
6.3.1 Wiring Check	III.6-12
6.3.2 Voltage Check	III.6-13
6.3.2.1 Domestic	III.6-13
6.3.2.2 International	III.6-17
6.3.3 Voltage Selector Switch Check	III.6-22
6.3.4 Safety Warning Label Check	III.6-22
6.4 Power Up	III.6-23

7 Running Diagnostics

7.1 Overview	III.7-1
7.2 Processor Diagnostics	III.7-1
7.3 Channel Control Unit Diagnostics	III.7-3
7.4 Multibus Input/Output Processor Diagnostics	III.7-4
7.5 VMEbus Input/Output Processor Diagnostics	III.7-5

8 Installing System Software

8.1 Overview	III.8-1
8.2 Booting CONVEX UNIX	III.8-1
8.3 Installing CONVEX UNIX	III.8-2
8.4 Running sysex	III.8-2

9 Returning Equipment

9.1 Overview	III.9-1
9.2 Checking the Inventory	III.9-1
9.3 Packing the Cabinet	III.9-3
9.3.1 Tools	III.9-4
9.3.2 Placing the Cabinet on the Pallet	III.9-5

Appendixes**A Power and AC Specifications**

A.1 Overview	III.A-1
A.2 Equipment Dimensions	III.A-1
A.3 CONVEX Computer's Domestic Specifications	III.A-3
A.4 Equipment, Domestic Specifications	III.A-4
A.5 CONVEX Computer's International Specifications	III.A-6
A.6 Equipment, International Specifications	III.A-6
A.7 CONVEX Computer's Cooling Requirements	III.A-8
A.8 Equipment Cooling Requirements	III.A-8

B Reporting Problems

B.1 Overview	III.B-1
B.2 Information Required to Report a Problem	III.B-1

List of Tables

5-1 NEC Disk Drive Address Switch Bits	III.5-22
7-1 Processor Diagnostics	III.7-2
7-2 CCU Diagnostics	III.7-3
7-3 MIOP Diagnostics	III.7-4
7-4 VIOP Diagnostics	III.7-5
A-1 Equipment Dimensions and Weights	III.A-2
A-2 CONVEX Computer's Domestic Specifications	III.A-3
A-3 Equipment, Domestic Specifications	III.A-5
A-4 CONVEX Computer's International Specifications	III.A-6
A-5 Equipment, International Specifications	III.A-7
A-6 Computer Dissipation and Air Conditioning Requirements	III.A-8
A-7 Equipment Dissipation and Air Conditioning Requirements	III.A-9

List of Figures

2-1 Cabinet Power Label Location	III.2-2
2-2 Cabinet Power Label with "L" and "/" Symbols	III.2-3
2-3 Power Cord Caution Labels	III.2-5
2-4 Processor Cabinet Power Cord Labels	III.2-6
2-5 Expansion Cabinet Power Cord Labels	III.2-7
2-6 Location of Processor Cabinet Circuit Breaker	III.2-8
2-7 Location of Expansion Cabinet Circuit Breaker	III.2-9
2-8 Stabilizer Bars and Caution Label	III.2-10
3-1 Sales Order Packing Slip	III.3-2
3-2 Cabinet Packaging	III.3-4
3-3 Cabinet Pallet, Ramp and Auxiliary Ramp	III.3-5
3-4 C210/C220 Processor Cabinet and Pallet	III.3-6
4-1 Bulkhead Mounting Bracket and Shielded Cables	III.4-3

4-2 Cable Connections from Module to Backplane	III.4-5
4-3 Cabinet Connecting Brackets	III.4-6
5-1 Expansion Cabinet Power Controller	III.5-3
5-2 Stabilizer Bars and Caution Label	III.5-5
5-3 Multibus Chassis Shipping Carton	III.5-6
5-4 Multibus Controller Cable Routing	III.5-8
5-5 Multibus Cabling — Controllers to Rear Panel	III.5-10
5-6 Multibus Cabling to Disk and Tape Peripheral Devices	III.5-12
5-7 Stabilizer Bars and Caution Label	III.5-15
5-8 NEC Disk Drive Cable Connections	III.5-16
5-9 Rotary Actuator Locking/Unlocking	III.5-17
5-10 Peripheral Device Slide Rails	III.5-19
5-11 Non-Daisy-Chained Disk Drive Cabling	III.5-21
5-12 NEC Disk Drive Address Switches	III.5-23
5-13 Eagle Disk Drive Address Switch	III.5-24
5-14 Daisy-Chained Disk Drive Cabling	III.5-25
5-15 Expansion Cabinet Power Controller	III.5-27
6-1 AC Power Cord Conductor Configuration (Domestic)	III.6-8
6-2 AC Power Cord Conductor Configuration (International)	III.6-10
6-3 Power Controller Indicator Panels	III.6-15
6-4 Input AC Power Filter Studs (Domestic)	III.6-16
6-5 Power Controller Indicator Panels	III.6-19
6-6 Input AC Power Filter Studs (International)	III.6-20
9-1 CONVEX Shipper Request Form	III.9-2
9-2 Cabinet Pallet, Ramp and Auxiliary Ramp	III.9-4
9-3 C1 Processor Cabinet and Pallet	III.9-5
B-1 Sample <i>contact</i> Session	III.B-3

Volume IV CONVEX General Maintenance Guide

1 Safety Considerations

1.1 Overview	IV.1-1
1.2 Electrical Safety Precautions	IV.1-1
1.3 Electrostatic Discharge Precautions	IV.1-2
1.4 Thermal Safety Precautions	IV.1-2
1.5 Mechanical Safety Procedures	IV.1-2

2 Preventive Maintenance

2.1 Overview	IV.2-1
2.2 Periodic Maintenance Schedule	IV.2-1
2.3 Processor Cabinet	IV.2-3
2.3.1 Fans and Filters	IV.2-3
2.3.1.1 Tools	IV.2-3
2.3.1.2 Door Filters	IV.2-4
2.3.1.3 Floor Air Filter Location	IV.2-5
2.3.2 Processor Power Supply Voltages	IV.2-6
2.3.2.1 Tools	IV.2-7
2.3.2.2 Processor Power Supplies	IV.2-8
2.4 Multibus Chassis	IV.2-10
2.4.1 Multibus Fans and Filters	IV.2-10
2.4.2 Multibus Power Supply Voltages	IV.2-12
2.5 VMEbus Chassis	IV.2-12
2.5.1 VMEbus Fans and Filters	IV.2-12
2.5.2 VMEbus Power Supply Voltages	IV.2-13
2.6 System Disks	IV.2-14
2.6.1 Disk Drive Line Blower and Filter	IV.2-14
2.6.2 Disk Drive Power Supply Voltages	IV.2-15
2.7 Cipher Cartridge Tape	IV.2-15
2.8 Tape Drives	IV.2-15
2.8.1 Tape Path	IV.2-15
2.8.1.1 Beginning of Tape/End of Tape	IV.2-16
2.8.1.2 Tape Drive Tape Cleaner Block	IV.2-16
2.8.1.3 Tape Drive Read/Write Head Skew	IV.2-16
2.8.1.4 Tape Drive Supply Hub	IV.2-17
2.8.2 Reel Servo Operating Levels	IV.2-18
2.8.3 Capstan Velocity and Ramps	IV.2-18
2.8.4 File Protect Mechanism	IV.2-18
2.8.5 Read Output Amplitudes	IV.2-18
2.8.6 Rewind Operations	IV.2-19
2.8.7 Pneumatics	IV.2-19
2.8.7.1 Drive Belts	IV.2-19
2.8.7.2 Pneumatics Levels	IV.2-19
2.8.8 Tape Drive Fans	IV.2-20
2.8.9 Tape Drive Indicators	IV.2-20
2.8.10 Tape Drive Voltages	IV.2-21
2.8.10.1 2920 Tape Drive	IV.2-21
2.8.10.2 1960 Tape Drive	IV.2-21
2.8.11 Tape Drive Internal Diagnostics	IV.2-22
2.9 Printronix Printer	IV.2-22
2.9.1 Printer Assemblies	IV.2-23

2.9.2 Power Supply	IV.2-23
2.9.3 Printer Fans and Filters	IV.2-24
2.9.4 Printer Quality	IV.2-24
2.9.5 Lubrication	IV.2-24
3 Software	
3.1 Overview	IV.3-1
3.2 Error Messages	IV.3-1
3.2.1 Error Message Files	IV.3-1
3.2.2 Error Message Formats	IV.3-2
3.2.2.1 Error Log Messages	IV.3-2

Appendixes

A Test Equipment and Special Tools	
A.1 Overview	IV.A-1
A.2 Special Tools	IV.A-1
B Problem Reporting	
B.1 Overview	IV.B-1
B.2 Information Required to Report a Problem	IV.B-1

List of Tables

2-1 Periodic Hardware Maintenance	IV.2-2
2-2 Periodic Software Maintenance	IV.2-3
2-3 Power Supply Voltages	IV.2-9
2-4 Multibus Chassis Voltages and Tolerances	IV.2-12
2-5 VMEbus Voltages and Tolerances	IV.2-14
2-6 Eagle Disk Drive Voltages and Tolerances	IV.2-15
2-7 Pneumatics Levels	IV.2-20
2-8 2920 Tape Drive Voltages and Tolerances	IV.2-21
2-9 1960 Tape Drive Voltages	IV.2-22
2-10 Printronix Printer Voltages	IV.2-23

List of Figures

1-1 Stabilizer Bars and Caution Label	IV.1-3
2-1 Door Filter and Latches	IV.2-4
2-2 Floor Air Filter Location	IV.2-5
2-3 Power Supplies Location	IV.2-7
2-4 Multibus Air Filter	IV.2-11
2-5 VMEbus Chassis Air Filter	IV.2-13
B-1 Sample <i>contact</i> Session	IV.B-3

Volume V CONVEX Troubleshooting Guide

1 Introduction

1.1 Overview	V.1-1
1.2 CONVEX C200 Series Troubleshooting Philosophy	V.1-1
1.3 C2 Troubleshooting Methodology	V.1-2

2 System Dead

2.1 Overview	V.2-1
2.2 AC Power Bad	V.2-1
2.3 Power Supply Circuit Breaker Tripped	V.2-1
2.4 SCM Shut Down	V.2-1

3 Fails During Boot

3.1 Overview	V.3-1
3.2 Introduction	V.3-1
3.3 C200 Boot Processes	V.3-3
3.4 Power OFF to Front Panel	V.3-3
3.4.1 System Power Up	V.3-4
3.4.2 Power-On Self-Test (POST)	V.3-4
3.4.3 Front Panel	V.3-4
3.5 Fails During Power OFF to Front Panel Transition	V.3-5
3.5.1 Fails During Powerup	V.3-5
3.5.2 Fails During POST	V.3-6
3.6 Front Panel to SPU UNIX	V.3-6
3.7 Fails During SPU UNIX Boot	V.3-6
3.7.1 SP2 Cannot Access Boot Device	V.3-7
3.7.2 SPU Hangs or Crashes During Boot	V.3-8
3.7.3 SPU UNIX Panics	V.3-8
3.8 SPU UNIX to CONVEX UNIX	V.3-8
3.8.1 System Initialization	V.3-9
3.8.1.1 Control Stores	V.3-9
3.8.1.2 System Memory Configuration	V.3-9
3.8.1.3 I/O Configuration File	V.3-10
3.8.1.4 CONVEX UNIX <i>init</i>	V.3-10
3.8.1.5 Program Counter	V.3-10
3.8.2 Booting the CONVEX UNIX Kernel	V.3-10
3.9 Fails During CONVEX UNIX Boot	V.3-11
3.9.1 Fails During System Initialization	V.3-11
3.9.1.1 <i>spu4000</i>	V.3-11
3.9.1.2 <i>sysreset</i>	V.3-12
3.9.1.3 <i>mminit</i>	V.3-13
3.9.2 Fails During UNIX Kernel Execution	V.3-13

4 Fails During UNIX Process Execution

4.1 Overview	V.4-1
4.2 UNIX Processes	V.4-1
4.3 Fails During SPU UNIX Process	V.4-1
4.4 Fails During CONVEX UNIX Process	V.4-2
4.4.1 Hang	V.4-2
4.4.2 UNIX Crash	V.4-2
4.5 Hard Error Crash	V.4-2

4.6 Wrong Answer	V.4-2
4.7 Wrong Answer/Core Dump	V.4-2
5 Fails Diagnostics	
5.1 Overview	V.5-1
5.2 Troubleshooting With Diagnostic Tests Flowchart	V.5-1
5.3 CONVEX C200 Diagnostic Tests	V.5-2
5.3.1 CPU Diagnostic Tests	V.5-2
5.3.1.1 Isolation of Functional Blocks	V.5-3
5.3.1.2 Running Diagnostic Tests	V.5-3
5.3.1.3 Interpretation of Diagnostic Test Failures	V.5-3
5.3.2 Machine Malfunctions	V.5-1
5.3.2.1 System Failures	V.5-4
5.3.2.2 Wrong Answer	V.5-5
5.4 Troubleshooting With Diagnostics	V.5-6
5.4.1 Diagnostic Tests Do Not Fail	V.5-6
5.4.1.1 Intermittent System Failures	V.5-6
5.4.1.2 Repeatable System Failure; All Diagnostic Tests Pass	V.5-7
5.4.2 Diagnostic Tests Fail Intermittently	V.5-7
5.4.3 Diagnostic Tests Fail Repeatably	V.5-7
5.4.3.1 Revision Level Incompatibility	V.5-8
5.4.3.2 Design Problem	V.5-9
5.4.3.3 Failed Hardware	V.5-9
5.4.4 Repair Verification	V.5-10
6 Indicators	
6.1 Overview	V.6-1
6.2 Introduction	V.6-1
6.3 System Control Module (SCM)	V.6-1
6.3.1 Pre-Power Up	V.6-2
6.3.2 Power Up	V.6-3
6.3.3 Normal Monitoring	V.6-4
6.3.3.1 AC Power	V.6-4
6.3.3.2 DC Voltage Levels	V.6-5
6.3.3.3 Current Load Sharing	V.6-5
6.3.3.4 Air Temperatures	V.6-6
6.3.3.5 Internal Airflow	V.6-6
6.3.3.6 Fan Operation	V.6-6
6.4 Front Panel and Door Panel Indicators	V.6-7
6.4.1 ATTENTION	V.6-8
6.4.2 POWER	V.6-8
6.4.3 RUN	V.6-8
6.4.4 REMOTE	V.6-9
6.4.5 LOCAL	V.6-9
6.5 Power Controller Indicators	V.6-10
6.5.1 Phase Indicator Lights	V.6-13
6.5.2 Power Supply Indicator Lights	V.6-13
6.6 SCM Error Codes (System Status Display)	V.6-14
6.6.1 SCM Error Codes — Quick Reference	V.6-15
6.6.2 SCM Error Codes — Defined	V.6-17

7 Hard Error Messages

7.1 Overview	V.7-1
7.2 Hard Error Messages	V.7-1
7.2.1 ASP Hard Errors	V.7-2
7.2.2 CPX Hard Errors	V.7-7
7.2.3 DCU Hard Errors	V.7-21
7.2.4 IPP Hard Errors	V.7-27
7.2.5 MCM Hard Errors	V.7-32
7.2.6 PIA Hard Errors	V.7-35
7.2.7 VPC Hard Errors	V.7-39
7.2.8 VPD Hard Errors	V.7-44

8 I/O Error Messages

8.1 Overview	V.8-1
8.2 I/O Error Message List	V.8-2
8.3 I/O Error Messages	V.8-17
8.3.1 CPU side of Ethernet Driver — 1	V.8-17
8.3.2 CPU side of Ethernet Driver — 2	V.8-17
8.3.3 VIOP EGOS Messages	V.8-19
8.3.4 CPU side of UD	V.8-19
8.3.5 HE Driver on HSP	V.8-19
8.3.6 CPU Side of Multibus TTY Driver	V.8-21
8.3.7 CPU Side of Console Driver	V.8-21
8.3.8 CPU Side of Multibus Disk Driver	V.8-21
8.3.9 CPU Side of Multibus Raw Hyperchannel Driver	V.8-22
8.3.10 CPU Side of Multibus Internet Hyperchannel Driver	V.8-22
8.3.11 CPU Side of Multibus DR11W Driver	V.8-23
8.3.12 CPU Side of Driver Support Routines	V.8-24
8.3.13 CPU Side of Multibus Printer Driver	V.8-24
8.3.14 CPU Side of Multibus Plotter Driver	V.8-25
8.3.15 CPU Side of Multibus Tape Driver	V.8-25
8.3.16 IOP Side of Multibus TTY Driver	V.8-26
8.3.17 IOP Side of Multibus Disk Driver (Xylogics)	V.8-27
8.3.18 IOP Side of Ethernet Driver	V.8-28
8.3.19 IOP Side of Raw Hyperchannel Driver	V.8-31
8.3.20 IOP Side of Hyperchannel Internet Driver	V.8-31
8.3.21 IOP Side of Multibus Printer Driver	V.8-31
8.3.22 IOP Side of Multibus Plotter Driver	V.8-32
8.3.23 IOP Side of Multibus Tape Driver	V.8-32
8.3.24 Special IOP Side of EGOS <i>proc_dev</i> Command	V.8-32
8.3.25 IOP Side Driver Support Routines	V.8-33
8.3.26 CPU Side of VIOP (Interphase) Disk Driver	V.8-33
8.3.27 CPU Side of VME (VTAPE) Tape Driver	V.8-34
8.3.28 VIOP Side of SMD and ESDI Disk Driver	V.8-34
8.3.29 VIOP Side of VME Tape Driver	V.8-36
8.3.30 VIOP Side of UWDD UD Driver	V.8-37
8.3.31 VME Ethernet Driver	V.8-37
8.3.32 VIOP Side Driver Support Routines	V.8-39
8.3.33 VIOP EGOS Messages	V.8-39
8.3.34 CCU EGOS Messages	V.8-41
8.3.35 HSP EGOS Messages	V.8-42
8.3.36 MIOP EGOS Messages	V.8-44
8.3.37 MIOP EGOS Messages	V.8-45

8.3.38 IOP Internal Errors V.8-45
 8.3.39 VIOP Internal Errors V.8-47

9 SPU UNIX Messages

9.1 Overview V.9-1
 9.2 Troubleshooting SPU UNIX Error Messages Flowchart V.9-1
 9.3 SPU UNIX Messages V.9-1

10 CONVEX UNIX Messages

10.1 Overview V.10-1
 10.2 Troubleshooting CONVEX UNIX Error Messages Flowchart V.10-1
 10.3 CONVEX UNIX Panic Messages V.10-1
 10.4 CONVEX UNIX/HSP Panic Messages V.10-32
 10.5 CONVEX UNIX/IOP Panic Messages V.10-33
 10.6 CONVEX UNIX/VIOP Panic Messages V.10-35

Appendixes

A Crash Dump Procedure

A.1 Crash Dump Procedure V.A-1

B CPU Instruction Glossary

B.1 Overview V.B-1
 B.2 CPU Instruction Glossary V.B-1

C ASP Entry Point Listing

C.1 Overview V.C-1
 C.2 ASP Entry Points — by Entry Points V.C-2
 C.3 ASP Entry Points — by Opcode V.C-21

D Wire Lists

E Reporting Problems

E.1 Overview V.E-1
 E.2 Information Required to Report a Problem V.E-1

List of Tables

1-1 Failure Modes V.1-3
 6-1 SCM Temperature Trip Points V.6-6
 6-2 SCM Error Codes — Quick Reference V.6-15
 8-1 Common Print Formats V.8-2
 8-2 I/O Error Message Source Key V.8-3
 8-3 I/O Error Message List V.8-4

List of Figures

3-1 Boot Processes V.3-2
 6-1 System Control Module V.6-2
 6-2 SCM-to-Indicator Cabling V.6-7
 6-3 Power Controller AC Distribution (Domestic) V.6-11
 6-4 Power Controller AC Distribution (International) V.6-12
 7-1 ASP #100 data flow V.7-2

7-2 ASP #101 data flow	V.7-3
7-3 ASP #102 data flow	V.7-4
7-4 ASP #103 data flow	V.7-5
7-5 CPX #400 data flow	V.7-7
7-6 CPX #401 data flow	V.7-8
7-7 CPX #402 data flow	V.7-9
7-8 CPX #403 data flow	V.7-10
7-9 CPX #404 data flow	V.7-11
7-10 CPX #405 data flow	V.7-12
7-11 CPX #406 data flow	V.7-13
7-12 CPX #407-#411 data flow	V.7-14
7-13 CPX #412 data flow	V.7-15
7-14 CPX #417/#418 data flow	V.7-16
7-15 CPX #419 data flow	V.7-17
7-16 CPX #420 data flow	V.7-18
7-17 CPX #421 data flow	V.7-19
7-18 CPX #422 data flow	V.7-20
7-19 DCU #200 data flow	V.7-21
7-20 DCU #201 data flow	V.7-23
7-21 DCU #202 data flow	V.7-24
7-22 DCU #203 data flow	V.7-25
7-23 DCU #204/205 data flow	V.7-26
7-24 IPP #300 data flow	V.7-27
7-25 IPP #301 data flow	V.7-28
7-26 IPP #302 data flow	V.7-29
7-27 IPP #303 data flow	V.7-30
7-28 IPP #304 data flow	V.7-31
7-29 MCM #500 data flow	V.7-32
7-30 MCM #501 data flow	V.7-34
7-31 PIA #601 data flow	V.7-36
7-32 PIA #602 data flow	V.7-37
7-33 VPC #700 data flow	V.7-39
7-34 VPC #701 data flow	V.7-40
7-35 VPC #702 data flow	V.7-41
7-36 VPC #703 data flow	V.7-42
7-37 VPC #704 data flow	V.7-43
7-38 VPD #800 data flow	V.7-44
7-39 VPD #801 data flow	V.7-45
7-40 VPD #802 data flow	V.7-46
7-41 VPD #803/#804 data flow	V.7-47
E-1 Sample <i>contact</i> Session	V.E-3

Volume VI CONVEX Removal/Replacement Guide

1 Introduction

1.1 Overview	VI.1-1
1.2 Safety	VI.1-1
1.3 Returned Parts	VI.1-1
1.4 Factory Repair	VI.1-1
1.5 Replacement of Parts	VI.1-1
1.6 Parts Ordering	VI.1-2

2 Safety Considerations

2.1 Overview	VI.2-1
2.2 Electrical Safety Precautions	VI.2-1
2.3 Electrostatic Discharge Precautions	VI.2-1
2.4 Thermal Safety Precautions	VI.2-2
2.5 Mechanical	VI.2-2

3 Returned Item Documentation

3.1 Overview	VI.3-1
3.2 <i>PART & ASSEMBLY FAILURE REPORT</i>	VI.3-1
3.2.1 Preliminary Information	VI.3-3
3.2.2 Failure Mode Description	VI.3-7
3.2.3 System Configuration	VI.3-10
3.2.4 Intermittent Failures	VI.3-11
3.2.5 Multibus/VMEbus Voltages	VI.3-13
3.2.6 Sample <i>PART & ASSEMBLY FAILURE REPORT</i>	VI.3-13
3.3 Test Tag	VI.3-15

4 Removal and Replacement

4.1 Overview	VI.4-1
4.2 Removal & Replacement Preliminaries	VI.4-1
4.2.1 Power Up	VI.4-2
4.2.2 Power Down	VI.4-4
4.3 AC Power	VI.4-5
4.3.1 AC Power Cord Disconnection	VI.4-8
4.3.2 AC Power Cord Connection	VI.4-8
4.4 Cabinet	VI.4-8
4.4.1 Door	VI.4-8
4.4.1.1 Tools	VI.4-10
4.4.1.2 Removal	VI.4-10
4.4.1.3 Installation	VI.4-10
4.4.2 Door Indicator Circuit Board	VI.4-10
4.4.2.1 Tools	VI.4-11
4.4.2.2 Removal	VI.4-11
4.4.2.3 Installation	VI.4-12
4.4.3 Door Air Filter	VI.4-12
4.4.3.1 Tools	VI.4-14
4.4.3.2 Removal	VI.4-14
4.4.3.3 Installation	VI.4-14
4.4.4 Side Panel	VI.4-14
4.4.4.1 Tools	VI.4-15
4.4.4.2 Removal	VI.4-15

4.4.4.3	Installation	VI.4-15
4.4.5	Rear Panel	VI.4-16
4.4.5.1	Tools	VI.4-16
4.4.5.2	Removal	VI.4-16
4.4.5.3	Installation	VI.4-16
4.4.6	Front Control Panel Assembly	VI.4-16
4.4.6.1	Tools	VI.4-17
4.4.6.2	Removal	VI.4-18
4.4.6.3	Installation	VI.4-18
4.4.7	Front Control Panel Printed Circuit Board	VI.4-18
4.4.7.1	Tools	VI.4-18
4.4.7.2	Removal	VI.4-18
4.4.7.3	Installation	VI.4-19
4.4.8	Floor Air Filter	VI.4-19
4.4.8.1	Tools	VI.4-19
4.4.8.2	Removal	VI.4-20
4.4.8.3	Installation	VI.4-20
4.5	Processor Cards	VI.4-20
4.5.1	Tools	VI.4-21
4.5.2	Removal	VI.4-22
4.5.3	Installation	VI.4-23
4.6	Processor Card Foreplane Connector	VI.4-24
4.6.1	Tools	VI.4-26
4.6.2	Removal	VI.4-26
4.6.3	Installation	VI.4-26
4.7	Lower Bay	VI.4-26
4.7.1	Lower Bay Cover and Lower Air Plenum	VI.4-27
4.7.1.1	Tools	VI.4-27
4.7.1.2	Removal	VI.4-28
4.7.1.3	Installation	VI.4-28
4.7.2	SPU Disk Drive	VI.4-29
4.7.2.1	Tools	VI.4-30
4.7.2.2	Removal	VI.4-30
4.7.2.3	Installation	VI.4-31
4.7.3	SPU Tape Drive	VI.4-32
4.7.3.1	Tools	VI.4-33
4.7.3.2	Removal	VI.4-33
4.7.3.3	Installation	VI.4-35
4.7.4	SPU Tape Paddle Board	VI.4-35
4.7.4.1	Tools	VI.4-35
4.7.4.2	Removal	VI.4-35
4.7.4.3	Installation	VI.4-36
4.7.5	System Control Module	VI.4-36
4.7.5.1	Tools	VI.4-38
4.7.5.2	Removal	VI.4-38
4.7.5.3	Installation	VI.4-38
4.7.6	Power Controller	VI.4-39
4.7.6.1	Tools	VI.4-40
4.7.6.2	Removal	VI.4-40
4.7.6.3	Installation	VI.4-45
4.7.7	Intake Air Temperature Sensor	VI.4-47
4.7.7.1	Tools	VI.4-47
4.7.7.2	Removal	VI.4-47

4.7.7.3 Installation	VI.4-47
4.8 Cooling	VI.4-48
4.8.1 Lower and Upper Rear Plenum	VI.4-48
4.8.1.1 Tools	VI.4-49
4.8.1.2 Removal	VI.4-49
4.8.1.3 Installation	VI.4-50
4.8.2 Fan Assembly	VI.4-50
4.8.2.1 Tools	VI.4-53
4.8.2.2 Removal	VI.4-53
4.8.2.3 Installation	VI.4-53
4.8.3 Fan Subassembly	VI.4-54
4.8.3.1 Tools	VI.4-55
4.8.3.2 Removal	VI.4-55
4.8.3.3 Installation	VI.4-55
4.8.4 Fan Assembly Airflow Sensors	VI.4-55
4.8.4.1 Tools	VI.4-55
4.8.4.2 Removal	VI.4-55
4.8.4.3 Installation	VI.4-56
4.8.5 Fan Assembly Exhaust Temperature Sensor	VI.4-56
4.8.5.1 Tools	VI.4-56
4.8.5.2 Removal	VI.4-56
4.8.5.3 Installation	VI.4-56
4.9 Card Cage	VI.4-57
4.9.1 Tools	VI.4-57
4.9.2 Removal	VI.4-57
4.9.3 Installation	VI.4-58
4.10 Backplane and Backplane Connector Pins	VI.4-59
4.10.1 Backplane	VI.4-59
4.10.1.1 Tools	VI.4-59
4.10.1.2 Removal	VI.4-59
4.10.1.3 Installation	VI.4-61
4.10.2 Backplane Connector Pin	VI.4-64
4.10.3 Backplane Connector Pin (Standard)	VI.4-66
4.10.3.1 Tools	VI.4-67
4.10.3.2 Removal	VI.4-67
4.10.3.3 Installation	VI.4-67
4.10.4 Backplane Connector Pin (Short)	VI.4-68
4.10.4.1 Tools	VI.4-69
4.10.4.2 Removal	VI.4-69
4.10.4.3 Installation	VI.4-69
4.10.5 Backplane Connector Pin (Insulated)	VI.4-70
4.10.6 Sense Board	VI.4-70
4.10.6.1 Tools	VI.4-71
4.10.6.2 Removal	VI.4-71
4.10.6.3 Installation	VI.4-71
4.11 DC Power	VI.4-72
4.11.1 Power Supply	VI.4-72
4.11.1.1 Tools	VI.4-73
4.11.1.2 Removal	VI.4-73
4.11.1.3 Installation	VI.4-74
4.11.2 Powerplane	VI.4-75
4.11.2.1 Tools	VI.4-75
4.11.2.2 Removal	VI.4-76

4.11.2.3 Installation VI.4-77

5 Illustrated Parts Breakdown

5.1 Overview VI.5-1
 5.2 How to Use the Parts List VI.5-1
 5.3 Mechanical Illustrated Parts Breakdown VI.5-4
 5.3.1 Front Cabinet Assemblies VI.5-4

Appendixes

A Part Number Identification

A.1 Overview VI.A-1
 A.2 Production Numbers VI.A-1
 A.3 Marketing Numbers VI.A-20

B Reporting Problems

B.1 Overview VI.B-1
 B.2 Information Required to Report a Problem VI.B-1

List of Tables

4-1 Sense Board to Backplane Connections VI.4-70
 5-1 Sample Parts List VI.5-3
 5-2 C2 Door Parts List VI.5-4
 5-3 Front Cabinet Parts List VI.5-6
 5-4 Intake Plenum Parts List VI.5-8
 5-5 Control Panel Parts List VI.5-10
 5-6 Lower Bay Parts List VI.5-12
 5-7 Power Controller (Domestic) Parts List VI.5-14
 5-8 Power Controller (International) Parts List VI.5-16
 5-9 SPU Disk Parts List VI.5-18
 5-10 SPU Peripherals Parts List VI.5-20
 5-11 System Control Module Parts List VI.5-22
 5-12 Rear Cabinet Parts List VI.5-24
 5-13 Exhaust Plenum Parts List VI.5-26
 5-14 Fans Parts List VI.5-28
 5-15 Board Set Parts List VI.5-30
 A-1 Part Number Assignment Codes VI.A-1
 A-2 Part Number Family Descriptions VI.A-15

List of Figures

3-1 *PART & ASSEMBLY FAILURE REPORT* VI.3-2
 3-2 Preliminary Information VI.3-4
 3-3 Failure Mode Information VI.3-7
 3-4 System Configuration Information VI.3-10
 3-5 Intermittent Failure Information VI.3-11
 3-6 Multibus/VMEbus Voltage Information VI.3-13
 3-7 Sample *PART & ASSEMBLY FAILURE REPORT* VI.3-14
 3-8 Test Tag VI.3-16
 3-9 CONVEX Board Flow Diagram VI.3-17
 4-1 Power Indicators VI.4-2
 4-2 Location of Processor Cabinet Circuit Breaker VI.4-6

4-3 AC Power Cord Connectors	VI.4-7
4-4 Door and Pivot Pin	VI.4-9
4-5 Door Indicator Circuit Board	VI.4-11
4-6 Door Air Filters	VI.4-13
4-7 Panel Quick Release Latches	VI.4-15
4-8 Front Control Panel Assembly	VI.4-17
4-9 Processor Cards	VI.4-21
4-10 Card Cage Cover	VI.4-22
4-11 Foreplane Connector	VI.4-25
4-12 Lower Air Plenum	VI.4-27
4-13 SPU Disk	VI.4-30
4-14 SPU Disk Jumper	VI.4-31
4-15 SPU Tape Drive	VI.4-33
4-16 SPU Tape Jumper	VI.4-34
4-17 System Control Module	VI.4-37
4-18 Power Controller Connectors	VI.4-41
4-19 Power Controller Indicator Panel	VI.4-42
4-20 Power Controller AC Power Input Stud Configuration	VI.4-43
4-21 Power Controller	VI.4-44
4-22 Lower Rear Plenum	VI.4-49
4-23 Upper Rear Plenum	VI.4-50
4-24 Fan Assembly	VI.4-52
4-25 Backplane Pins	VI.4-65
4-26 Backplane Standard Pin	VI.4-66
4-27 Backplane Short Pins	VI.4-68
4-28 Power Supplies	VI.4-73
5-1 Sample Parts Breakdown	VI.5-3
5-2 C2 Door Parts Breakdown	VI.5-5
5-3 Front Cabinet Parts Breakdown	VI.5-7
5-4 Intake Plenum Parts Breakdown	VI.5-9
5-5 Front Control Panel Parts Breakdown	VI.5-11
5-6 Lower Bay Parts Breakdown	VI.5-13
5-7 Power Controller (Domestic) Parts Breakdown	VI.5-15
5-8 Power Controller (Int'l) Parts Breakdown	VI.5-17
5-9 SPU Disk Parts Breakdown	VI.5-19
5-10 Spu Peripherals Parts Breakdown	VI.5-21
5-11 System Control Module Parts Breakdown	VI.5-23
5-12 Rear Cabinet Parts Breakdown	VI.5-25
5-13 Exhaust Plenum Parts Breakdown	VI.5-27
5-14 Fans Parts Breakdown	VI.5-29
5-15 Board Set Parts Breakdown	VI.5-31
B-1 Sample <i>contact</i> Session	VI.B-3

Chapter 3

Master Index

3.1 Overview

This chapter contains the master index to the six volumes that comprise the *CONVEX Maintenance Documentation* kit.

THIS PAGE INTENTIONALLY LEFT BLANK

Master Index

Numeric

1960 tape drive, power supply voltages IV.2-21
2920 tape drive, power supply voltages IV.2-21
2's Complement Number System II.1-2
32-Bit Load, Illustrated II.5-25
64-Bit Load, Illustrated II.5-26
64-Bit TOC Clock, Illustrated II.2-51
8-Bit Load, Illustrated II.5-25

A

A register. *See* Address register
AC power III.6-1
AC Power VI.4-5
AC Power Bad V.2-1
AC power, cabling III.5-26
AC power, connections III.6-1, III.6-2
AC power, connections, domestic III.6-2
AC power, connections, international III.6-9
AC power connectors III.2-4
AC power cord, connection VI.4-8
AC power cord connectors, illustrated VI.4-7
AC power cord, disconnection VI.4-8
AC power cord labels III.2-4
AC power, hard-wired connections, domestic III.6-6
AC power plug, connecting III.6-6
AC power, power check III.6-11
AC power receptacle, attaching, domestic III.6-3
AC Power, SCM V.6-4
AC power, sources III.6-3
AC power, voltage check III.6-13
AC power, voltage check, domestic III.6-13
AC power, voltage check, international III.6-17
AC power, wiring check III.6-12
AC power-controller, defined I.4-1
Access mode, defined I.4-1
Accessing Stack Resource Structure, Illustrated II.2-32
Accounting, *etc/group* II.A-11
Accumulator, defined I.4-1
Active CPU Base-Level Processing II.2-47
Active CPU Interrupt Level Processing II.2-48
Active CPU Interrupt Processing II.2-47
Adding New Users, *etc/nurc* II.A-14
Address and Data Crossbar II.5-14
Address, defined I.4-1
Address, Lengths II.1-2
Address Mapping, Communication Register, Table II.2-11
Address Mapping, Physical Communication, Illustrated II.2-10
Address register, defined I.4-1
Address Registers II.1-2
Address scalar processor, defined I.4-1
Address space, defined I.4-1
Address translation fault, defined I.4-1
Address Translation Faults II.1-4
Address Translation Unit (ATU) II.1-3
Address translation unit, defined I.4-1
Address, Unsigned Values II.1-2
Addressing, Communication Register II.2-7
Addressing mode, defined I.4-2
Address/Scalar Processor Subsystem II.1-11
Address/Scalar Unit Functions, Table II.1-11
Agent, defined I.4-2
Air Temperatures, SCM V.6-6
Align (IPP) II.3-16
Alignment and Partials II.6-24
Alpha Addressing II.3-25
Alpha Addressing, Table II.3-25
Alpha8 Addressing, Table II.3-25
ALU Function Pipe Micro Control II.4-18
ALU Function Pipe Write Control II.4-19
ALU Pipe Compare Operations II.B-7
ALU Pipe Reduction Operations II.B-7
ALU Pipe Vector Result Operations II.B-6
ALU Pipeline II.4-17
ALU Pipeline Functions, Table II.4-17
ALU. *See* Arithmetic logic unit

Arbitration and Crossbar Gate Arrays II.7-4
Arbitration Considerations II.6-22
Arbitration Controller II.5-12
Architecture, defined I.4-2
Architecture, For Memory Management II.1-3
Architecture Overview II.2-1
Argument pointer, defined I.4-2
Arithmetic and Logic Unit (ASP) II.3-4
Arithmetic Exceptions, New II.2-34
Arithmetic logic unit, defined I.4-2
Arrays II.1-2
Arrays, defined I.4-2
ASAP, Multiprocessing II.2-20
ASAP. *See* Automatic Self-Allocating Processors
ASP #100 data flow, Block Diagram V.7-2
ASP #101 data flow, Block Diagram V.7-3
ASP #102 data flow, Block Diagram V.7-4
ASP #103 data flow, Block Diagram V.7-5
ASP Entry Point Listing V.C-1
ASP Entry Point Listing - by Entry Points V.C-2
ASP Entry Point Listing - by Opcode V.C-21
ASP Entry Point Listing - Overview V.C-1
ASP Hard Errors V.7-2
ASP. *See* Address scalar processor
Associated documentation, listed I.xi, I.1-3, III.xi, IV.xi
Associated documentation, ordering I.xiii, I.1-3, III.xii
Asymmetric Parallel Processing, Illustrated II.2-22
ATF. *See* Address translation fault
ATTENTION, Indicator V.6-8
ATU. *See* Address translation unit
Automatic Self-Allocating Processors II.2-20

B

b. *See* Byte
Backplane VI.4-59
Backplane connector pin VI.4-64
Backplane connector pin damage, caution VI.4-20
Backplane connector pin, insulated VI.4-70
Backplane connector pin, short VI.4-68
Backplane connector pin, short, installation VI.4-69
Backplane connector pin, short, removal VI.4-68
Backplane connector pin, standard VI.4-66
Backplane connector pin, standard, installation VI.4-67
Backplane connector pin, standard, removal VI.4-67
Backplane, defined I.4-2
Backplane, installation VI.4-61
Backplane pins, illustrated VI.4-65
Backplane pins, short, illustrated VI.4-68
Backplane, removal VI.4-59
Bandwidth II.5-22
Base-Level Interrupt, Returning from II.2-48
Basic Booting Procedures II.1-37
BBUS Arbitration Control, Table II.3-3
BBUS Control (SFU) II.3-2
Beginning of Tape/End of Tape, reflector IV.2-16
Beginning of Tape/End of Tape, sensor IV.2-16
Billing, *etc/group* II.A-11
Binary License, Library Files II.1-42
Bit complement, defined I.4-2
Bit, defined I.4-2
Block, defined I.4-2
Board Level Control II.7-14
Board set VI.5-30
Board Set Revision Level V.5-8
Boldface, for user-entered information I.x, III.x, IV.x
Boot, defined I.4-2
Boot Processes Block Diagram V.3-1
Bootting CONVEX UNIX, in Multi-user Mode II.1-40
Bootting From Power-Up To CONVEX UNIX Multi-User Mode II.1-40
Bootting in Diagnostic Mode II.1-41
Bootting SPU UNIX, Table II.1-41
Bootting the CONVEX UNIX Kernel V.3-10
Bootting the system, CONVEX UNIX III.8-1
Bootting the system, SPU UNIX III.7-1
Bourne Shell II.1-37
Brackets, for optional entries I.x, III.x, IV.x
Branch Address Register (IPP) II.3-16

Master Index

Branch, defined I.4-2
Branches II.3-7
Breakpoint, defined I.4-2
Bus Acquisition II.6-21
Bus Arbitration II.6-21
Bus Lock II.6-22
Bus Release II.6-21
Byte II.1-2
Byte, defined I.4-2
Byte Validity (DCU) II.3-23

C

C, defined I.4-3
C Shell II.1-37
C shell, defined I.4-3
C130, C210, C220 System Diagnostics, Release Notice
I.1-3
C2 door VI.5-4
C2 door Parts breakdown VI.5-5
C2 Troubleshooting Methodology V.1-2
C200 Boot Processes V.3-3
Cabinet VI.4-8
Cabinet connecting brackets, illustrated III.4-6
Cabinet, Description II.1-5
Cabinet, Expansion II.1-7
Cabinet installation, new system III.0
Cabinet installation, system upgrade III.5-1
Cabinet packaging, illustrated III.3-3, III.3-5
Cabinet packaging, removing III.3-5
Cabinet power labels III.2-1
Cabinet, Processor II.1-5
Cabinet stabilizer bars III.2-9
Cabinet stabilizer bars, illustrated IV.1-2
Cabinets, cabling III.4-1
Cabinets, securing III.4-6
Cable connections, Multibus III.4-5
Cabling, AC power III.5-26
Cabling, cabinets III.4-1
Cabling, disk drives, daisy chained III.5-24
Cabling, disk drives, discussed III.5-21
Cabling, disk drives, non-daisy chained III.5-21
Cabling, modem III.4-2
Cabling, Multibus III.4-4
Cabling, Multibus controller cables III.5-7
Cabling, power sequencing cable III.4-6, III.5-26
Cabling, terminal III.4-2
Cabling, VMEbus Input/Output Processor III.4-5,
III.5-26
Cache Consistency II.2-5
Cache, defined I.4-3
Cache purge, defined I.4-3
Cache. *See also* Instruction cache; Logical cache; Physical
cache
Capacity II.5-20
Capstan assembly, alignment IV.2-16
Capstan ramps IV.2-18
Capstan velocity and ramps IV.2-18
Card cage VI.4-57
Card cage cover, illustrated VI.4-22
Card cage, installation VI.4-58
Card cage, removal VI.4-57
CCU Domain II.1-24
CCU. *See* Channel Control Unit
CCU Subsystem Functional Diagram II.1-23
Central Processing Unit II.1-3
Central processing unit, defined I.4-3
Certification restrictions III.2-4
cfork Instruction II.2-26
Chaining, defined I.4-3
Channel Control Unit II.6-27
Channel control unit, cable mounting brackets, illustrated
III.4-2
Channel Control Unit (CCU) II.1-23
Channel control unit, diagnostics III.7-3
Channels, Interrupt II.2-41
Chassis, defined I.4-3
Checking equipment AC power ratings III.2-1

Checking input power III.2-4
Cipher cartridge tape IV.2-15
Cipher cartridge tape, head assembly, cleaning IV.2-15
CIR Division, Communication Register, Illustrated II.2-8
CIR Logical-to-Physical Mapping, Illustrated II.2-9
Circuit Breaker Tripped, Power Supply V.2-1
Claims, damage, reporting III.3-3
Clock Generation Logic II.4-23, II.6-16
Clock Generator II.5-17
cnvxhwdoc, electronic mailbox, for reader comments
I.xiii, I.1-4, II.xviii, III.xii, IV.xi, V.xiv, VI.xiii
Command Interpreters II.1-37
Communication Register Address Mapping, Table II.2-11
Communication Register Addressing II.2-7
Communication Register CIR Division, Illustrated II.2-8
Communication Register Modified Bits II.2-17
Communication Registers II.2-7, II.7-12
Communication Registers, Fork Event II.2-14
Communication Registers, Hardware II.2-12
Communication Registers, Hardware, Illustrated II.2-12
Communication Registers, Hardware Reserved II.2-13
Communication Registers, Hardware Reserved, Illustrated
II.2-14
Communication Registers, Memory Structures Locked
with II.2-18
Compare Operations, ALU Pipe II.B-7
Compiler, defined I.4-3
Complex II.1-3
Connectors, power III.2-4
contact, for reporting problems II.C-1, III.B-1, IV.B-1,
V.E-1, VI.B-1
Context Bits II.3-17
Control panel
Control Stores, loading V.3-9
Control System, Interrupt II.2-43
CONVEX Computer Site Preparation Guide I.xi, III.xi
CONVEX Architecture Reference I.1-3
CONVEX C100/C200 Series PBUS Structure, Illustrated
II.6-21
CONVEX C200 Diagnostic Tests V.5-2
CONVEX C200 Series Troubleshooting Philosophy V.1-1
CONVEX Computer Site Preparation Guide (C200 Series)
I.1-3
*CONVEX Diagnostic Database (C130, C210, C220),
Release Notice* I.1-3
CONVEX Diagnostic Documentation (C200 Series) I.xi,
I.1-3, III.xi
CONVEX HIA User's Guide I.1-3
CONVEX Operating System II.1-24
CONVEX Processor Operation Guide I.xi, I.1-3, III.xi
CONVEX Removable Disk System Operation Guide I.xi,
I.1-3, III.xi
CONVEX Shipper Request form, illustrated III.9-1
CONVEX System Manager's Guide I.1-3
CONVEX UNIX, booting III.8-1
CONVEX UNIX, Booting to Multi-user Mode II.1-40
CONVEX UNIX Command Interpreters II.1-37
CONVEX UNIX, defined I.4-3
CONVEX UNIX, Description II.1-36
CONVEX UNIX *init* V.3-10
CONVEX UNIX, installation III.8-1
CONVEX UNIX Kernel, Booting the V.3-10
CONVEX UNIX Messages, Overview V.10-1
CONVEX UNIX Multi-user, Description of II.1-40
CONVEX UNIX Panic Messages V.10-1
CONVEX UNIX, Release Notice I.1-3
CONVEX UNIX/HSP Panic Messages V.10-32
CONVEX UNIX/IOP Panic Messages V.10-33
CONVEX UNIX/VIOP Panic Messages V.10-35
CONVEX VIOP/VBCU Service Guide I.xi, I.1-3, III.xi
Cooling VI.4-48
Cooling requirements, CONVEX computers, defined
III.A-8
Cooling requirements, peripheral equipment, defined
III.A-8
CPU Diagnostic Tests V.5-2
CPU Domain II.1-24
CPU Execution Clock Registers II.2-16
CPU Execution Timer II.2-52
CPU Execution Timers, Illustrated II.2-52

CPU Functional Block Diagram II.1-8
 CPU Instruction Glossary V.B-1
 CPU Instruction Glossary - Overview V.B-1
 CPU Instruction Processor (IP) Functional Block Diagram II.1-13
 CPU Interrupt Arbiter II.7-13
 CPU Memory Interface (MI) Functional Block Diagram II.1-14
 CPU Scalar Processor (SP) Functional Block Diagram II.1-12
 CPU. *See* Central processing unit
 CPU Utility Unit II.7-3
 CPU Utility Unit (CPX) II.1-31
 CPU Utility Unit (CPX) Functional Block Diagram II.1-31
 CPU Vector Processor (VP) Subsystem Functional Block Diagram II.1-16
 CPX #400 data flow, Block Diagram V.7-7
 CPX #401 data flow, Block Diagram V.7-8
 CPX #402 data flow, Block Diagram V.7-9
 CPX #403 data flow, Block Diagram V.7-10
 CPX #404 data flow, Block Diagram V.7-11
 CPX #405 data flow, Block Diagram V.7-12
 CPX #406 data flow, Block Diagram V.7-13
 CPX #407-#411 data flow, Block Diagram V.7-14
 CPX #412 data flow, Block Diagram V.7-15
 CPX #418 data flow, Block Diagram V.7-16
 CPX #419 data flow, Block Diagram V.7-17
 CPX #420 data flow, Block Diagram V.7-18
 CPX #421 data flow, Block Diagram V.7-19
 CPX #422 data flow, Block Diagram V.7-20
 CPX Functional Block Diagram II.7-4
 CPX Hard Errors V.7-7
 CPX. *See* CPU Utility Unit
 Crash, CONVEX UNIX V.4-2
 Crash Dump Procedure V.A-1
 Crash, Hard Error V.4-2
 CTR Manipulation II.2-53
 Current Load Sharing, SCM V.6-5
 Customer support, telephone numbers for I.xiii, I.1-4, III.xii

D

d. *See* double
 Damage, shipping, discussed III.3-3
 Damage, shipping, reporting III.3-3
 Data Alignment II.1-2
 Data Cache (ASP, DCU, SFU) II.3-20
 Data cache unit, defined
 Data Crossbar II.5-14
 Data Flow Gate Arrays (ASP) II.3-20
 Data path, VME Subsystem, Defined II.6-28
 Data path, VME Subsystem, Illustrated II.6-28
 Data Representations II.1-2
 Data Transfer II.6-25
 Data type, defined I.4-3
 DC Power, power supplies VI.4-72
 DC Voltage Levels, SCM V.6-5
 Dcache Control (DCU) II.3-24
 Dcache Data (ASP) II.3-21
 Dcache Operations (ASP, DCU, SFU) II.3-22
 Dcache Operations, Table II.3-22
 Dcache Tags II.3-21
 DCU #200 data flow, Block Diagram V.7-21
 DCU #201 data flow, Block Diagram V.7-23
 DCU #202 data flow, Block Diagram V.7-24
 DCU #203 data flow, Block Diagram V.7-25
 DCU #204/205 data flow, Block Diagram V.7-26
 DCU Hard Errors V.7-21
 DCU. *See* Data cache unit
 DE. *See* Disk enclosure
 Deadlock Detection Instructions, Table II.2-36
 Deadlocks II.2-36
dead.report, contact file II.C-2, III.B-2, IV.B-2, V.E-2, VI.B-2
 Design Problems, Troubleshooting V.5-9
 Destination, defined I.4-3

Device Domain II.1-24
 Diagnostic Interface II.1-28
 Diagnostic Test Categories, CONVEX C200 Series V.5-2
 Diagnostic Test Failures, Interpretation of V.5-3
 Diagnostic Tests, CONVEX C200 Series V.5-2
 Diagnostic Tests Do Not Fail, Troubleshooting When V.5-6
 Diagnostic Tests Fail Intermittently, Troubleshooting V.5-7
 Diagnostic Tests Fail Repeatably, Troubleshooting V.5-7
 Diagnostic Tests, Running V.5-3
 Diagnostics II.1-31
 Diagnostics, channel control unit III.7-3
 Diagnostics, Multibus Input/Output Processor III.7-4
 Diagnostics, processor III.7-1
 Diagnostics, tape drive, internal IV.2-22
 Diagnostics, VMEbus Input/Output Processor III.7-5
 Directory paths, italicizing I.x, III.x, IV.x
 Disk Description File, */etc/disktab* II.A-3
 Disk drive, fans IV.2-14
 Disk drive, filters IV.2-14
 Disk drive, line blower IV.2-14
 Disk drive, power supply voltages IV.2-15
 Disk drives, cabling, daisy chained III.5-24
 Disk drives, cabling, discussed III.5-21
 Disk drives, cabling, non-daisy chained III.5-21
 Disk error messages IV.3-2
 Disk head, locking, illustrated III.5-17
 Disk Partitions, Striped II.A-6, II.A-27
disktab File II.A-3
 Displacement, defined I.4-3
 Divide Function Unit Control II.4-21
 Divide Operations, Multiply Pipe II.B-8
 DIVX Divide and Square Root (SFU) II.3-5
 DIVX Function Throughput Times, Table II.4-20, II.4-21
 DMA. *See* Direct memory access
 DMM. *See* Digital multimeter
 Document numbers, format, in preface I.xiii, I.1-3, III.xii
 Documents, ordering, how to I.xiii, I.1-3, III.xii
 Door VI.4-8
 Door air filter VI.4-12
 Door air filter, installation VI.4-14
 Door air filter, removal VI.4-14
 Door and pivot pin, illustrated VI.4-9
 Door and pivot pin, installation VI.4-10
 Door and pivot pin, removal VI.4-10
 Door indicator circuit board VI.4-10
 Door indicator circuit board, figure VI.4-10
 Door indicator circuit board, installation VI.4-12
 Door indicator circuit board, removal VI.4-11
 Double Precision, Longword II.1-2

E

EARB Internals II.6-6
 EARB/PBUS Arbiter Interface II.6-5
 EARB/Return Queue Interface II.6-6
 EARB/SP2 Interface II.6-6
 EBUS Arbiter II.6-5
 EBUS Arbitration II.6-4
 EBUS, defined I.4-3
 EBUS Description II.1-22, II.6-3
 EBUS Interface II.6-4
 ECC. *See* Error checking and correction
 Eight-Way Interleaving of One MCM Pair, Illustrated II.5-21
 Electrical specifications, domestic III.A-1
 Electromagnetic interference shielding, illustrated III.4-2
 Electronic mailbox, for reader comments I.xiii, I.1-4, II.xviii, III.xii, IV.xi, V.xiv, VI.xiii
 Electronic mailbox, for reader comments, what to include in I.xiii, I.1-4, II.xviii, III.xii, IV.xii, V.xiv, VI.xiii
 Electrostatic discharge, defined I.4-4
 Electrostatic Discharge, servicing precautions III.2-12
 Electrostatic discharge, servicing precautions IV.1-2
 Electrostatic Discharge, servicing precautions VI.2-1
 EMI. *See* Electromagnetic interference

Master Index

- Emphasis, *italics* for I.x, III.x, IV.x
Environment Monitoring II.7-21
Error Codes Defined, System Status Display (SCM) V.6-17
Error Codes, System Status Display (SCM) — Quick Reference Table V.6-15
Error Handling II.6-14
Error message files, discussed IV.3-1
Error message files, formats IV.3-2
Error Message List, I/O, table V.8-4
Error Messages Defined: ASP Hard Errors V.7-2
Error Messages Defined: CONVEX UNIX Panic Messages V.10-1
Error Messages Defined: CONVEX UNIX/HSP Panic Messages V.10-32
Error Messages Defined: CONVEX UNIX/IOP Panic Messages V.10-33
Error Messages Defined: CONVEX UNIX/VIOP Panic Messages V.10-35
Error Messages Defined: CPX Hard Errors V.7-7
Error Messages Defined: DCU Hard Errors V.7-21
Error Messages Defined: IPP Hard Errors V.7-27
Error Messages Defined: MCM Hard Errors V.7-32
Error Messages Defined: PIA Hard Errors V.7-35
Error Messages Defined: SPU UNIX V.9-1
Error Messages Defined: VPC Hard Errors V.7-39
Error Messages Defined: VPD Hard Errors V.7-44
Error messages, discussed IV.3-1
Error messages, disk IV.3-2
Error messages, error log, formats IV.3-2
Error Messages, I/O V.8-2
Error Messages, I/O defined V.8-17
Error Messages, I/O Overview V.8-1
Error Messages, I/O Source Key table V.8-3
Error messages, magnetic tape IV.3-2
Errors II.6-25
ESD. *See* Electrostatic Discharge
ESD. *See* Electrostatic discharge
Essential System Files II.1-43
Essential System Files, Overview II.A-1
/etc/disktab II.A-3
/etc/fstab II.A-5
/etc/gettytab II.A-7, II.A-31
/etc/group II.A-11
/etc/hosts II.A-12
/etc/nurc II.A-14
/etc/passwd II.A-16
/etc/phones II.A-25
/etc/printcap II.A-18
/etc/pwrestrict II.A-21
/etc/rc.local II.A-23
/etc/remote II.A-24
/etc/securetty II.A-26
/etc/stripecap II.A-27
/etc/tapecap II.A-29
/etc/tty5 II.A-31
/etc/ttytype II.A-33
/etc/utmp II.A-31
Europe, technical assistance, how to obtain I.xiii, I.1-4, III.xii
Even Memory Bus, Illustrated II.5-3
Even Memory, Illustrated II.5-2
Exception, defined I.4-4
Exception, Invalid Communication Address II.2-35
Exceptions II.1-4
Executive mode, defined I.4-4
Exhaust plenum VI.5-26
Expansion cabinet, defined I.4-4
Extended Opcodes II.2-2
-
- F**
- FAD Control States, Table II.3-4
FAD Fast Adder (IPP) II.3-4
Failed Hardware, Troubleshooting V.5-9
Fails Diagnostics, Overview V.5-1
Fails During Boot: Introduction V.3-1
Fails During Boot: Overview V.3-1
Fails During CONVEX UNIX Boot V.3-11
Fails During CONVEX UNIX Process V.4-2
Fails During POST V.3-6
Fails During Power OFF to Front Panel Transition V.3-5
Fails During Powerup V.3-5
Fails During SPU UNIX Boot V.3-6
Fails During SPU UNIX Process V.4-1
Fails During System Initialization V.3-11
Fails During UNIX Kernel Execution V.3-13
Fails During UNIX Process Execution, Overview V.4-1
Failure Categories V.1-2
Failure Modes, Table V.1-2
Fan assembly VI.4-50
Fan assembly airflow sensor VI.4-55
Fan assembly airflow sensor, installation VI.4-56
Fan assembly airflow sensor, removal VI.4-55
Fan assembly exhaust temperature sensor VI.4-56
Fan assembly exhaust temperature sensor, installation VI.4-56
Fan assembly exhaust temperature sensor, removal VI.4-56
Fan assembly, illustrated VI.4-51
Fan assembly, installation VI.4-53
Fan assembly, removal VI.4-53
Fan Operation, SCM V.6-6
Fan subassembly VI.4-54
Fan subassembly, installation VI.4-55
Fan subassembly, removal VI.4-55
Fans assembly VI.5-28
Fans, disk drive line blower IV.2-14
Fans, multibus IV.2-10
Fans, printer IV.2-24
Fans, processor cabinet IV.2-3
Fans, processor power supply IV.2-3
Fans, tape drives IV.2-20
Fans, VMEbus IV.2-12
Fault, defined I.4-4
Fault States, Saving II.3-30
Faults II.3-12, II.3-29
Faults, Processor Status Words II.4-15
FCU. *See* Formatter/control unit
FIFO. *See* Queue
File protect mechanism, tape drives IV.2-18
File System, Static Information File, /etc/fstab II.A-5
Filenames, italicizing I.x, III.x, IV.x
Files, Essential System II.A-1
Files, System II.A-1
Filters, disk drive IV.2-14
Filters, multibus IV.2-10
Filters, Multibus, illustrated IV.2-10
Filters, printer IV.2-24
Filters, processor IV.2-3
Filters, processor, door IV.2-4
Filters, processor, door, illustrated IV.2-4
Filters, processor, floor, illustrated IV.2-5
Filters, VMEbus IV.2-12
Filters, VMEbus chassis, illustrated IV.2-12
Firmware, defined I.4-4
First-in, first-out. *See* Queue
Fixed Point Integers, 2's Complement Number System II.1-2
Fixed Point Integers, Summary II.1-2
Flag, defined I.4-4
Floating Point Arithmetic, IEEE II.1-2
Floating Point Arithmetic, Native II.1-2
Floating Point Arithmetic, Summary II.1-2
Floating point, defined I.4-4
Floor air filter VI.4-19
Floor air filter, installation VI.4-20
Floor air filter, removal VI.4-20
Forced faulting mode, defined I.4-4
Foreplane connector, illustrated VI.4-25
Foreplane connector, installation VI.4-26
Foreplane connector, removal VI.4-26
Fork Event Communication Registers II.2-14
Fork Event Registers, Illustrated II.2-23
Forking Instructions II.2-23
Forking, Multiprocessing II.2-20
FORTRAN, defined I.4-4

fp. *See* Front Panel
 Fraction, defined I.4-4
 Frame. *See* Page frame; Stack frame
 Front cabinet VI.5-6, VI.5-7
 Front control panel assembly VI.4-16
 Front control panel assembly, illustrated VI.4-17
 Front control panel assembly, installation VI.4-18
 Front control panel assembly, removal VI.4-18
 Front control panel printed circuit board VI.4-18
 Front control panel printed circuit board, installation VI.4-19
 Front control panel printed circuit board, removal VI.4-18
 Front Panel V.3-4
 Front Panel and Door Panel Indicators V.6-7
 Front Panel Indicators II.7-24
 Front Panel to SPU UNIX V.3-6
 fsck Program, /etc/fstab II.A-6
 fsck utility, defined I.4-4
 FSE. *See* Farside echo board
 fstab File II.A-5
 FUJITSU M2951A/AF Mini Disk Drive, Customer Engineering Manual I.1-3
 Function unit, defined I.4-5
 Function Unit Gate Array Operations, Table II.4-16
 Function Units II.1-19, II.4-16
 Functional Blocks, Isolation of V.5-3

G

Gate array, defined I.4-5
 Gather, defined I.4-5
 getlogin II.A-31
 getmntent Program, /etc/fstab II.A-6
 getty II.A-7, II.A-31
 gettytab File II.A-7
 group File II.A-11
 Guard bit, defined I.4-5

H

h. *See* Halfword
 Halfword II.1-2
 Halfword, defined I.4-5
 Hang, System V.4-2
 Hard Error Conditions II.6-14
 Hard Error Crash V.4-2
 Hard Error Messages V.7-1
 Hard Error Messages, Overview V.7-1
 Hardware Components, C201, C202, C210, C220, Illustrated II.1-4
 Hardware/Software Relationships II.1-24
 Hazards II.3-17
 HDA. *See* Head disk assembly
 Header Longword II.6-22
 Header Longword, Illustrated II.6-23
 Host Name Database, /etc/hosts II.A-12
 hosts File II.A-12
 HSP. *See* High-speed parallel interface

I

Icache Memory Allocation, Table II.3-6
 Icache. *See* Instruction cache
 Icache Valid A and Valid B (IPP) II.3-11
 Idle CPU Interrupt Processing II.2-46
 Idle Loop, Microcode II.2-27
 idle Sk Instruction II.2-27
 IEC. *See* Electrotechnical Commission
 Illustrations, reference numbers I.x, III.x, IV.x
 Immediates, defined I.4-5
 Index, master, overview I.3-1
 Indexing, register, defined I.4-5
 Indicator: V.6-8
 Indicator: ATTENTION V.6-8

Indicator: LOCAL V.6-9
 Indicator: REMOTE V.6-9
 Indicator: RUN V.6-8
 Indicator: System Status Display (SCM Error Codes) V.6-14
 Indicators, Front Panel and Door Panel V.6-7
 Indicators, Introduction V.6-1
 Indicators, Overview V.6-1
 Indicators: Phase V.6-13
 Indicators: Power Controller V.6-10
 Indicators: Power Supply V.6-13
 Indicators, tape drives IV.2-20
 Indirection, defined I.4-5
 info(1), man page II.C-1, III.B-1, IV.B-1, V.E-1, VI.B-1
 init Program II.A-31
 Initialization Traps II.2-35
 Input Staging II.4-12
 Input Staging Pipeline, Illustrated II.4-8
 Input Staging to the VRF, Illustrated II.4-12
 Input/output processor, defined I.4-5
 Input/Output Subsystem, Overview II.6-1
 Installation, cabinets, system upgrade III.5-27
 Installation, cabling III.4-1
 Installation, new system III-0
 Installation Procedure, CONVEX UNIX and Utilities I.1-3
 Installation, software III.8-2
 Instruction II.4-16
 Instruction cache, defined I.4-5
 Instruction Cache (IPP) II.3-6
 Instruction, defined I.4-5
 Instruction Dispatch II.3-7
 Instruction Dispatch Control II.1-19
 Instruction Glossary, CPU V.B-1
 Instruction Lookahead II.3-10
 Instruction Processor II.1-12, II.3-5
 Instruction processor unit, defined
 Instructions, Deadlock Detection, Table II.2-36
 Instructions, Forking II.2-23
 Intake air temperature sensor VI.4-47
 Intake air temperature sensor, installation VI.4-47
 Intake air temperature sensor, removal VI.4-47
 Intake plenum VI.5-7
 Integers, Fixed Point. *See* Fixed Point Integers
 Interleaving and Numeric Precision, Table II.5-21
 Interleaving, Memory II.5-21
 Interleaving of One MCM Pair, Eight-Way, Illustrated II.5-21
 Intermittent System Failures, Troubleshooting V.5-6
 Internal Airflow, SCM V.6-6
 International power requirements. *See* Power requirements III.A-6
 Interpretation of Diagnostic Test Failures V.5-3
 Interrupt Arbiter II.6-9
 Interrupt Arbitration II.6-9
 Interrupt, Base-Level, Returning from II.2-48
 Interrupt Bus Cycle II.6-26
 Interrupt Channels II.2-41
 Interrupt Context Block, Illustrated II.2-45
 Interrupt Context Blocks II.2-45
 Interrupt Control Register (ICR) II.2-42
 Interrupt Control Register (ICR), Illustrated II.2-42
 Interrupt Control System II.2-43
 Interrupt, defined I.4-5
 Interrupt Flow—C220, Illustrated II.2-43
 Interrupt Handling II.7-18
 Interrupt Interface II.6-9
 Interrupt Level Translation II.6-9
 Interrupt Processing II.2-41
 Interrupt Processing, General Information II.2-48
 Interrupt Signal Timing II.6-26
 Interrupt State machine II.6-9
 Interrupt Vector Assignment II.6-26
 Interrupts II.1-4, II.2-41, II.3-9, II.7-17
 Interrupts and Traps II.3-12
 Interrupts, base-level, defined I.4-2
 Interrupts, Processor Response II.1-4
 Interval Timer II.2-49, II.7-9
 Interval Timer Counter II.2-51
 Interval timer, defined I.4-5
 Interval Timer Format, Illustrated II.2-50

Master Index

Interval Timer Functional Diagram II.7-9
Interval Timer Interrupt Number II.2-51
Interval Timer Status Register II.2-50
Interval Timer Status Register, Illustrated II.2-50
Intrinsics II.2-3
Introduction, Fails During Boot V.3-1
Introduction, Indicators V.6-1
Introduction, Overview V.1-1
Invalid Communication Address Exception II.2-35
Inventory, checking III.3-1, III.9-1
I/O Access Ports II.7-3
I/O Configuration File V.3-10
I/O Data References, Mapped II.1-4
I/O Error Message List V.8-2
I/O Error Message List, table V.8-4
I/O Error Message Source Key, table V.8-3
I/O Error Messages, defined V.8-17
I/O Error Messages, Overview V.8-1
I/O Processor, Description of II.1-24
I/O Processor Subsystem Functional Diagram II.1-24
I/O Subsystem II.1-21
I/O Subsystem Functional Block Diagram II.1-21, II.6-1
IOP, Features List II.6-32
IOP. *See* Input/output processor
IPB assembly indexes, use of VI.5-2
IPB figure number, use of VI.5-1
IPB item number, use of VI.5-1
IPB overview VI.5-1
IPP #300 data flow, Block Diagram V.7-27
IPP #301 data flow, Block Diagram V.7-28
IPP #302 data flow, Block Diagram V.7-29
IPP #303 data flow, Block Diagram V.7-30
IPP #304 data flow, Block Diagram V.7-31
IPP Hard Errors V.7-27
IPP. *See* Instruction processor unit
ips. *See* Inches per second
Isolation of Functional Blocks V.5-3

J

join Instruction II.2-26
Jump Address Register (IPP) II.3-15
Jump, defined I.4-6
Jump Instruction Execution Times, Table II.3-15
Jumps II.3-7
Jumps That Cause Dispatch Lockup, Illustrated II.3-12

K

Kernel, defined I.4-6
Keypad, defined I.4-6

L

l. *See* Longword
ldcmr Instruction II.2-17
ldcmr Memory Map, Illustrated II.2-17
Library Files, Binary License II.1-42
Library Files, Source License II.1-42
Line blower, disk drive IV.2-14
Load, 32-Bit, Illustrated II.5-25
Load, 64-Bit, Illustrated II.5-26
Load, 8-Bit, Illustrated II.5-25
Load and Store Function Pipe Micro Control II.4-10
Load and Store Function Pipe Write Control II.4-11
Load, defined I.4-6
Load Vector Register II.B-1
Load Vector Register/Vector Index II.B-2
Load VL II.B-4
Load VM II.B-4
LOCAL, Indicator V.6-9
Logical address, defined I.4-6
Logical Address Registers (DCU) II.3-26
Logical Address Space II.1-2
Logical cache, defined I.4-6

Logical memory, defined I.4-6
Logical Memory, Operating System II.1-2
Logical Value, Unsigned II.1-2
Logical-to-Physical Address Translation (SFU, DCU) II.3-24
Logical-to-Physical Mapping For 1 CIR, Illustrated II.2-9
login Program II.A-33
Longword II.1-2
Longword Address Bits, Table II.3-24
Longword, defined I.4-6
Longword Resource Structure Format, Illustrated II.2-19
Lookahead Cache (IPP) II.3-11
Lookahead Valid A and Valid B (IPP) II.3-13
Lookaside Register (IPP) II.3-16
Look-Aside-Buffer (DCU, SFU) II.3-28
Lower air plenum, illustrated VI.4-27
Lower air plenum, installation VI.4-28
Lower air plenum, removal VI.4-28
Lower bay VI.4-26, VI.5-12
Lower bay cover and lower air plenum VI.4-27
Lower bay cover, installation VI.4-28
Lower bay cover, removal VI.4-28
Lower rear plenum VI.4-48
Lower rear plenum, illustrated VI.4-48
Lower rear plenum, installation VI.4-50
Lower rear plenum, removal VI.4-49

M

M, abbreviation, for mega I.x, III.x, IV.x
Machine exceptions, defined I.4-6
Machine Malfunctions V.5-4
Magnetic tape error messages IV.3-2
Main Memory Domain II.1-24
Main Memory Refresh Control II.1-28
Main memory. *See* Physical memory
Maintenance documentation, overview I.1-1
make depend, System Generation II.1-42
make install, System Generation II.1-43
make, System Generation II.1-42
MAM to MCM Configuration, Table II.5-20
Maskable interrupt, defined I.4-6
Master index. *See* Index, master
Master table of contents. *See* Table of contents, master
MBCU, in MIOP System II.1-24, II.6-32
MBCU. *See* Multibus control unit
Mbyte. *See* Megabyte
MCM #500 data flow, Block Diagram V.7-32
MCM #501 data flow, Block Diagram V.7-34
MCM Control I/O II.5-8
MCM Cycle Types, Table II.5-10
MCM Hard Errors V.7-32
MCM Memory Addressing in the Memory Subsystem, Illustrated II.5-24
MCM Memory Addressing, Table II.5-24
MCM Processor Port I/O II.5-8
MCM with 4 MAMs and 8 Banks of Memory, Illustrated II.5-7
Mechanical safety precautions VI.2-2
Mega, abbreviation for I.x, III.x, IV.x
Megabyte, defined I.4-6
Memory II.3-28
Memory Access, 32-Bit II.5-25
Memory Access, 64-Bit II.5-26
Memory Access, 8-Bit II.5-25
Memory Address Paths, Illustrated II.3-18
Memory Addressing II.5-23
Memory and Scalar Processor Interface II.1-18, II.4-9
Memory Array Module (MAM) II.5-10
Memory Bank II.5-10
Memory Chip Size to MAM Population, Table II.5-20
Memory Contentions II.5-23
Memory Control (DCU) II.3-27
Memory Control Module (MCM) II.5-6
Memory Control Path II.6-4
Memory Cycle Types II.5-9
Memory Data Layout, Table II.3-14
Memory Data Path II.6-3

Memory Data Register (IPP) II.3-14
 Memory Duals of Communication Register Operations II.2-19
 Memory Fault Operation II.B-10
 Memory Interface II.1-14, II.3-18
 Memory Interleaving II.5-21
 Memory Loading II.5-24
 Memory management, defined I.4-6
 Memory Management, Summary II.1-2
 Memory Management Unit, Summary II.1-2
 Memory Management, Virtual II.2-4
 Memory Organization, Logical, Page 0, Illustrated II.2-31
 Memory Protection System II.1-3
 Memory Return Control (SFU) II.3-28
 Memory Structures Locked with Communication Registers II.2-18
 Memory Subsystem II.1-19
 Memory Subsystem Bandwidth, Table II.5-22
 Memory Subsystem Functional Block Diagram II.1-19
 Memory Subsystem Functional Block Diagram, Illustrated II.5-1
 Memory Subsystem, Organization II.5-2
 Memory subsystem, Overview II.5-1
 MFU Pipeline II.4-19
 Microcode, defined I.4-6
 Microcode Idle Loop II.2-27
 Microcode Revision Level V.5-8
 MIOP, Features II.1-24, II.6-32
 MIOP, Overview II.1-24, II.6-32
 MIOP. *See* Multibus Input/Output Processor
 Miscellaneous Logic II.5-19
 Miscellaneous Logic and Error Detection II.7-14
mminit V.3-13
 MMU. *See* Memory Management Unit
 Modem, cabling III.4-2
 Modems, with *contact* II.C-1, III.B-1, IV.B-1, V.E-1, VI.B-1
 Modified Bits, Memory Management II.1-3
 Move Scalar to Vector Element II.B-3
 Move Vector Element/Scalar II.B-4
 MPS. *See* Memory Protection System
 Multibus, cable connections III.4-5
 Multibus, cabling III.4-4
 Multibus, cabling, controller cables III.5-7
 Multibus cardcage, defined I.4-7
 Multibus chassis IV.2-10
 Multibus control unit, defined I.4-7
 Multibus, controller cards, installation III.5-7
 Multibus controller, defined I.4-7
 Multibus, defined I.4-6
 Multibus, fans IV.2-10
 Multibus, filters IV.2-10
 Multibus Input/Output Processor, diagnostics III.7-4
 Multibus, installation, upgrade III.5-4
 Multibus I/O Processor, Description of II.6-32
 Multibus packaging, illustrated III.5-6
 Multibus, power supply voltages IV.2-12
 Multibus, unpacking III.5-6
 Multiply Function Pipe Micro Control II.4-20
 Multiply Function Pipe Unit Control II.4-20
 Multiply Function Pipe Write Control II.4-21
 Multiply Operations, Multiply Pipe II.B-8
 Multiply Pipe Operations II.B-8
 Multiply Pipe Reduction Operations II.B-9
 Multiply Pipe Vector Edit Operations II.B-9
 Multiply Pipeline Operation Times, Table II.4-19
 Multiprocessing, Definition of II.1-4
 Multiprocessing (Forking/ASAP) II.2-20
 Multiprocessor Management II.1-3
 Multi-user mode, defined I.4-7

N

NCA Corporation standard descriptions VI.5-2
newfs Utility II.A-3
newst Utility II.A-3, II.A-27
 Next Interval Timer Count II.2-50
 Next Program Counter (ASP) II.3-16

nfs Systems Options, */etc/fstavg* II.A-5
 Normal Monitoring, SCM V.6-4
 Normal Operation II.7-21
 Notational conventions I.x, III.x, IV.x
 NRZI. *See* Non-return-to-zero-indicated
nu Defaults Database, */etc/nurc* II.A-14
nu Utility II.A-14, II.A-16, II.A-21
 Numeric Precision, Interleaving, Table II.5-21
nurc File II.A-14

O

Odd Memory Bus, Illustrated II.5-3
 Odd Memory, Illustrated II.5-2
 Opcodes, Extended II.2-2
 Operands, I/O, References II.1-4
 Operating System II.1-3
 Operating System, Call Processing II.1-3
 Operating System, CONVEX II.1-24
 Operating System, UNIX II.1-3
 Operating Systems II.1-30
 Operation States II.1-35
 Operations, Memory Duals of Communication Register II.2-19
 Operations, Primitive Communication Register II.2-16
 Order numbers, format, in preface I.xiii, I.1-3, III.xii
 Ordering documentation, how to I.xiii, I.1-3, III.xii
 Output Staging II.4-13
 Output Staging Pipeline, Illustrated II.4-13
 Overview, Fails Diagnostics V.5-1
 Overview: Fails During Boot V.3-1
 Overview, maintenance documentation I.1-1
 Overview, master index I.3-1
 Overview, master table of contents I.2-1
 Overview, problems, reporting II.C-1, III.B-1, IV.B-1, V.E-1, VI.B-1
 Overview, removal and replacement VI.4-1
 Overview: System Dead V.2-1

P

Packaging, removing, accessories III.3-8
 Packaging, removing, cabinet and pallet III.3-5
 Packing, C1 cabinet III.9-1
 Packing, C1 cabinet and pallet, illustrated III.9-5
 Packing material, saving III.3-3
 Page II.1-3
 Page 0 II.2-30
 Page 0 Logical Memory Organization, Illustrated II.2-31
 Page 0/Exceptions II.2-30
 Page 0/Traps II.2-30
 Page, defined I.4-7
 Page frame, defined I.4-7
 Page Frame, Memory Management II.1-3
 Page, Memory Management II.1-3
 Page table entry, defined I.4-7
 Page Table Entry (PTE), Memory Management II.1-3
 Page Tables, Memory Management II.1-3
 Pagefault, defined I.4-7
 Pages, Unencacheable II.2-6
 Panel quick release latches, illustrated VI.4-15
 Parallel Processing, Asymmetric, Illustrated II.2-22
 Parallel Processing, Symmetric, Illustrated II.2-21
 Parallelized Loop, Example II.2-29
 PART & ASSEMBLY FAILURE REPORT VI.3-1
 Part numbers. *See* Document numbers
 Partitioning, Trap Instruction Register, Illustrated II.2-38
passwd File II.A-16
passwd Utility II.A-21
 Password File, */etc/passwd* II.A-16
 Password Restrictions File, */etc/pwrestrict* II.A-21
pbkpt Instruction II.2-38
 PBUS Arbiter II.6-3
 PBUS Arbitration II.6-3
 PBUS Data Transfer Operations II.6-21
 PBUS, defined I.4-7

Master Index

- PBUS Description II.1-22
- PBUS, Description II.1-23
- PBUS Header Transfers II.6-10
- PBUS Interface II.6-2
- PBUS Interface Adapter II.6-2
- PBUS Interface Adapter (PIA) II.1-21
- PBUS Interface Capacity II.6-2
- PBUS Interrupts II.6-25
- PBUS Memory Base Pointer Read Transfer II.6-13
- PBUS Read Transfers II.6-12
- PBUS. *See* Peripheral Bus
- PBUS Signal Line Characteristics II.6-27
- PBUS Structure, CONVEX C100/C200 Series, Illustrated II.6-21
- PBUS TAM Transfers II.6-13
- PBUS Transaction Types, Table II.6-23
- PBUS Transactions II.6-22
- PBUS Write Transfers II.6-10
- PCB. *See* Printed circuit board
- PCU. *See* Physical cache unit
- Periodic maintenance schedule, hardware IV.2-1
- Periodic maintenance schedule, software IV.2-3
- Peripheral Bus II.6-20
- Peripheral equipment, specifications, domestic III.A-4
- Peripheral equipment, specifications, International III.A-6
- pfork <effa>*, Ak instruction II.2-25
- Phase Indicator Lights V.6-13
- Physical address, defined I.4-7
- Physical Address Mapping II.6-4
- Physical cache, defined I.4-7
- Physical Communication Address Mapping, Illustrated II.2-10
- Physical Configuration Map II.7-8
- Physical memory, defined I.4-7
- PIA #601 data flow, Block Diagram V.7-36
- PIA #602 data flow, Block Diagram V.7-37
- PIA Data Flow II.6-9
- PIA Hard Errors V.7-35
- PIA. *See* PBUS Interface Adapter
- PIA. *See* Peripheral bus interface adapter
- Pipeline, defined I.4-8
- Pneumatics, drive belts IV.2-19
- Pneumatics, levels, tape drive IV.2-19
- Pneumatics, tape drive IV.2-19
- Porting, defined I.4-8
- POST. *see* Power-Up Self-Test
- Post-Crack and Dispatch Register(IPP) II.3-17
- Power Bad, AC V.2-1
- Power controller VI.4-39
- Power Controller AC Distribution (Domestic), Illustration V.6-11
- Power Controller AC Distribution (International) V.6-12
- Power controller AC power input stud configuration, illustrated VI.4-43
- Power controller connectors, illustrated VI.4-40
- Power controller (domestic) VI.5-14
- Power controller, expansion cabinet, illustrated III.5-3, III.5-26
- Power controller, illustrated VI.4-44
- Power controller indicator panel, illustrated VI.4-42
- Power Controller Indicators V.6-10
- Power controller, installation VI.4-45
- Power controller (international) VI.5-16
- Power controller, removal VI.4-40
- Power cord voltage labels III.2-6
- Power Down II.1-35
- Power down, procedures VI.4-4
- Power Failure Sequencing II.7-22
- POWER, Indicator V.6-8
- Power indicators, illustrated VI.4-1
- Power Label Description III.2-2
- Power OFF to Front Panel V.3-3
- Power Requirements II.1-8
- Power requirements, maximum, domestic III.A-1
- Power requirements, maximum, international III.A-6
- Power requirements, minimum, domestic III.A-1
- Power requirements, minimum, international III.A-6
- Power sequencing cable, cabling III.4-6, III.5-26
- Power sources, delta vs. wye, connection to III.6-3
- Power Supplies II.7-23
- Power supplies, illustrated VI.4-73
- Power supply VI.4-72
- Power Supply Circuit Breaker Tripped V.2-1
- Power Supply Indicator Lights V.6-13
- Power supply, installation VI.4-74
- Power supply, processor, illustrated IV.2-6
- Power supply, removal VI.4-73
- Power supply voltages, 1960 tape drive IV.2-21
- Power supply voltages, 2920 tape drive IV.2-21
- Power supply voltages, disk drives IV.2-15
- Power supply voltages, Multibus IV.2-12
- Power supply voltages, printer IV.2-23
- Power supply voltages, processor IV.2-6
- Power supply voltages, tape drives IV.2-21
- Power supply voltages, VMEbus IV.2-13
- Power Up II.1-35
- Power up VI.4-2
- Power up, procedures III.6-23
- Power Up, SCM V.6-3
- Power-On Self-Test (POST) V.3-4
- Powerplane VI.4-75
- Powerplane, installation VI.4-77
- Powerplane, removal VI.4-76
- Power-up Procedures II.1-37
- Power-up Procedures, Table II.1-38
- Power-Up Sequence II.7-19
- Pre-Crack (IPP) II.3-14
- green* Program, /etc/fstap II.A-6
- Preliminaries, removal and replacement VI.4-1
- Pre-Power Up, SCM V.6-2
- Pre-power Up Sequence II.7-18
- Primitive Communication Register Operations II.2-16
- printcap* File II.A-18
- Printer assembly, cleaning IV.2-23
- Printer, cabinet, cleaning IV.2-23
- Printer, cam wick assembly IV.2-24
- Printer Capability Database, /etc/printcap II.A-18
- Printer, counterweight assembly IV.2-24
- Printer, counterweight shafts IV.2-24
- Printer, fans IV.2-24
- Printer, filters IV.2-24
- Printer, hammerbank assembly IV.2-23
- Printer, lubrication IV.2-24
- Printer, paper feed mechanism IV.2-23
- Printer, power supply voltages IV.2-23
- Printer, Printronix IV.2-22
- Printer quality, checking IV.2-24
- Printer, ribbon drive assembly IV.2-23
- Printer, shuttle assembly IV.2-23
- Printer, shuttle drive mechanism IV.2-23
- Printer, shuttle springs IV.2-24
- Printronix P6000 Maintenance Manual* I.1-3
- Problems, reporting II.C-1, III.B-1, IV.B-1, V.E-1, VI.B-1
- Process II.1-4
- Process Breakpoint II.2-38
- Process Deadlock Class Codes, Table II.2-38
- Process Deadlock Qualifiers, Table II.2-38
- Process, defined I.4-8
- Process exception, defined I.4-8
- Processing, Active CPU Base-Level II.2-47
- Processing, Active CPU Interrupt II.2-47
- Processing, Active CPU Interrupt Level II.2-48
- Processing, Idle CPU Interrupt II.2-46
- Processing, Interrupt II.2-41
- Processing, Interrupt, General Information II.2-48
- Processing, Parallel, Asymmetric, Illustrated II.2-22
- Processing, Parallel, Symmetric, Illustrated II.2-21
- Processor Cabinet Backplane—C201, C202, C210, C220, Illustrated II.1-6
- Processor cabinet circuit breaker, illustrated VI.4-5
- Processor cabinet, defined I.4-8
- Processor cabinet maintenance, discussed IV.2-3
- Processor card foreplane connector VI.4-24
- Processor card, installation VI.4-23
- Processor card, removal VI.4-22
- Processor cards VI.4-20
- Processor cards, illustrated VI.4-21
- Processor Diagnostics III.7-1
- Processor, filters, cleaning IV.2-3
- Processor Operation Environment II.1-35

Processor power supply, illustrated IV.2-6
 Processor, power supply voltages IV.2-6
 Processor Status Word (ASP) II.3-2
 Processor status word, defined I.4-8
 Processor Status Word (PSW), illustrated II.2-33
 Processor Status Word Register II.4-15
 Processor Status Words, Faults II.4-15
 Processor Trap Mechanism II.2-40
 Processor-to-Memory Control Priorities, Table II.3-27
 Program Counter V.3-10
 Program names, italicizing I.x, III.x, IV.x
 Programmable interrupt timer, defined I.4-8
 Protection, defined I.4-8
 Protection System, Design II.1-3
 PS. *See* Power supply
 PSW Bits, New II.2-33
 PSW. *See* Processor status word
 PSW. *See* Processor Status Word II.2-33
 PSW Traps, New II.2-33
 PTE Format II.2-6
 PTE Format, illustrated II.2-6
 PTE. *See* Page table entry
 PTE Violations, New II.2-34
 Publication titles, italicizing I.x, III.x, IV.x
putst Utility II.A-27
purestrict File II.A-21

Q

Queue, defined I.4-8

R

Ratings, outlets, utility III.2-1
rc.local File II.A-23
 Read, defined I.4-8
 Read Multiplexer II.5-17
 Read output amplitudes, tape drives IV.2-18
 Read Request to Even and Odd Memory, illustrated II.5-4
 Reader's Forum Lxiv, I.1-4, II.xix, III.xiii, IV.xii, V.xiv, VI.xiv
 Rear cabinet VI.5-24
 Rear panel VI.4-16
 Rear panel, installation VI.4-16
 Rear panel, removal VI.4-16
 Reduction Operations, ALU Pipe II.B-7
 Reduction Operations, Multiply Pipe II.B-9
 Reel servo, column vacuum sensors IV.2-18
 Reel servo, file reel null/gain IV.2-18
 Reel servo, machine reel null/gain IV.2-18
 Reel servo operating levels IV.2-18
 Reel servo, preliminary reels null IV.2-18
 Referenced and Modified Bits II.7-6
 Referenced Bits, Memory Management II.1-3
 Register, defined I.4-8
 Register File (ASP) II.3-2
 Register Sets II.1-2
 Registers, Partitioning II.1-2
remote File II.A-24
 Remote Host Description File, */etc/remote* II.A-24
 REMOTE, Indicator V.6-9
 Remote Invalidates II.2-5
 Removable Disk System, cabling III.4-6, III.5-26
 Repair Verification V.5-10
 Repeatable System Failure; All Diagnostic Tests Pass, Troubleshooting V.5-7
 Reporting problems I.xiii, I.1-4, II.xviii, III.xii, IV.xi, V.xiv, VI.xiii
 Requests to the Output Stage Controller, Table II.4-13
 Reset, defined I.4-8
 Restrictions, Virtual Memory Mapping II.2-46
 Return Queue II.6-7
 Returned item documentation VI.3-1
 Returning Equipment III.9-1
 Returning from a Base-Level Interrupt II.2-48
 Revision Level Incompatibility V.5-8

Revision sheet 3
 Rewind operations, tape drives IV.2-19
 Rings II.1-3
 Rings, defined I.4-8
 Root directory, defined I.4-8
 RUN, Indicator V.6-8
 Running Diagnostic Tests V.5-3
 Runtime, defined I.4-8

S

Safety IV.1-2
 Safety considerations, procedures for moving equipment III.2-1
 Safety precautions, electrical IV.1-1, VI.2-1
 Safety precautions, electrostatic discharge IV.1-2
 Safety precautions, thermal IV.1-2
 Sales Order Packing Slip, illustrated III.3-1
 SALU Conversions and Floating Point Subtraction (SFU) II.3-5
 Sample parts breakdown VI.5-3
 Sample parts list VI.5-3
 Saving Fault State II.3-30
 Scalar Extended Under Mask, Store II.B-3
 Scalar function unit, defined I.4-9
 Scalar Processor II.1-11
 Scalar Processor (SP) Overview II.3-1
 Scalar Processor Subsystem Functional Block Diagram II.3-1
 Scalar Registers II.1-2
 Scalar to Vector Element, Move II.B-3
 Scan Control II.5-17
 Scan Control Modes, Table II.5-9
 Scan Rings II.1-23
 SCM: AC Power V.6-4
 SCM: Air Temperatures V.6-6
 SCM Communications II.7-15
 SCM: Current Load Sharing V.6-5
 SCM: DC Voltage Levels V.6-5
 SCM Error Codes (System Status Display) V.6-14
 SCM: Fan Operation V.6-6
 SCM Hardware II.7-23
 SCM: Internal Airflow V.6-6
 SCM: Normal Monitoring V.6-4
 SCM: Power Up V.6-3
 SCM Power-Up Flow Diagram II.7-19
 SCM: Pre-Power Up V.6-2
 SCM Reads II.7-17
 SCM. *See* System control module
 SCM. *See* System Control Monitor
 SCM Shut Down V.2-1
 SCM Temperature Trip Points V.6-6
 SCM Writes II.7-17
 SCM-to-Indicator Cabling, illustration V.6-7
 Scratch RAM (ASP) II.3-3
 SCSI. *See* Small computer system interface
 SDR. *See* Segment descriptor register
securetty File II.A-26
 Securing, cabinets III.4-6
See
See Direct memory access controller, defined
 Segment, defined I.4-9
 Segment descriptor register, defined I.4-9
 Segment Descriptor Registers II.1-3, II.2-15
 Segmented ALU, defined I.4-9
 Sense board VI.4-70
 Sense board, installation VI.4-71
 Sense board, removal VI.4-71
 Service Processor Unit II.1-36
 Service Processor Unit 2 (SP2) II.1-25
 Service Processor Unit 2 (SP2) Functional Block Diagram II.1-26
 SFU. *See* Scalar function unit
 Shared Memory II.2-4
 Shift, defined I.4-9
 Shipping claims, reporting III.3-3
 Side panel VI.4-14
 Side panel, installation VI.4-15

Master Index

- Side panel, removal VI.4-15
- Single Precision, Word II.1-2
- Single(s), defined I.4-9
- SMB. *See* System monitor board
- SMD. *See* Storage module drives
- SMUL Multiplication (SFU) II.3-4
- Soft Error Conditions II.6-15
- Soft front panel, defined I.4-9
- Soft Front Panel, Description of II.1-36
- Soft Front Panel Firmware II.1-36
- Software III.7-1
- Software device driver, defined I.4-9
- Software installation III.8-2
- Software installation, CONVEX UNIX III.8-1
- Software/Hardware Relationships II.1-24
- Source License, Library Files II.1-42
- SP2 Cannot Access Boot Device V.3-7
- SP2 Command Sequencing, Illustrated II.7-16
- SP2 Communications II.7-15
- SP2 Connection II.1-23
- SP2 Diagnostic Interface II.1-23
- SP2 EBUS Interface II.1-28
- SP2 Hardware II.1-26
- SP2 Indicators II.1-27
- SP2 Peripherals II.1-29
- SP2 Read/TAM Transfers II.6-14
- SP2 Software II.1-30
- SP2 Write Transfers II.6-13
- spawn* <effa>, Ak Instruction II.2-26
- SPU III.7-1
- SPU Disk II.1-30
- SPU disk VI.5-18
- SPU disk drive VI.4-29
- SPU disk drive, installation VI.4-31
- SPU disk drive, removal VI.4-30
- SPU disk, illustrated VI.4-29
- SPU disk jumper, illustrated VI.4-31
- SPU Hangs or Crashes During Boot V.3-8
- SPU peripherals VI.5-20
- SPU. *See* Service Processor Unit
- SPU tape cartridge, defined I.4-9
- SPU Tape Drive II.1-30
- SPU tape drive VI.4-32
- SPU tape drive, defined I.4-9
- SPU tape drive, illustrated VI.4-32
- SPU tape drive, installation VI.4-35
- SPU tape drive, removal VI.4-33
- SPU tape jumper, illustrated VI.4-34
- SPU tape paddle board VI.4-35
- SPU tape paddle board, installation VI.4-36
- SPU tape paddle board, removal VI.4-35
- SPU UNIX, booting III.7-1
- SPU UNIX, Booting Procedures, Table II.1-41
- SPU UNIX, defined I.4-9
- SPU UNIX, Description II.1-36
- SPU UNIX Messages V.9-1
- SPU UNIX Messages, Overview V.9-1
- SPU UNIX Panics V.3-8
- SPU UNIX, Release Notice* I.1-3
- SPU UNIX to CONVEX UNIX V.3-8
- spu4000* V.3-11
- Square Root Operations, Multiply Pipe II.B-8
- Stack, defined I.4-9
- Stack Resource Structure Accessing, Illustrated II.2-32
- State Save and Restore Data II.1-19, II.4-23
- Static precautions III.2-12
- Status Registers II.1-2
- STC 1960 Series Tape Drive* I.1-3
- STC 2920 Tape Subsystem Maintenance Manual* I.1-3
- stcmr* Instruction II.2-17
- stcmr* Memory Map, Illustrated II.2-17
- Store Data Queue (ASP) II.3-29
- Store Scalar Extended Under Mask II.B-3
- Store using Vector Index II.B-3
- Store Vector Register II.B-2
- Store VM II.B-5
- stripecap* File II.A-27
- Striped Disk Partition Description Database, */etc/stripcap* II.A-27
- Striped Disk Partitions, */etc/fstab* II.A-6
- Sub-Complex II.1-3
- Supervisor, defined I.4-9
- Supply hub, tape drives IV.2-17
- Swappers II.3-24
- Symmetric Parallel Processing, Illustrated II.2-21
- sysex*. *See* System exerciser
- sysgen* II.1-41
- sysgen*, Description II.1-41
- sysreset* V.3-12
- System Architecture II.1-8
- System Clock Control II.1-28
- System Configurator V.5-8
- System Console II.1-29
- System console, defined I.4-10
- System control module VI.4-36, VI.5-22
- System control module, defined I.4-10
- System control module, illustrated VI.4-37
- System Control Module, Illustration V.6-1
- System control module, installation VI.4-38
- System control module, removal VI.4-38
- System Control Module (SCM) V.6-1
- System Control Monitor II.7-15
- System Control Monitor (SCM) II.1-33
- System Control Monitor (SCM) Functional Block Diagram II.1-33
- System Dead, Overview V.2-1
- System Descriptions II.1-4
- System exceptions, defined I.4-10
- System Exerciser, *sysex* III.8-2
- System Failures, Troubleshooting V.5-4
- System Faults II.3-29
- System Files II.A-1
- System Functional Block Diagram II.1-9
- System Generation, Description II.1-41
- System Generation, Library Files II.1-42
- System Generation, *make* II.1-42
- System Generation, *make depend* II.1-42
- System Generation, *make install* II.1-43
- System Generation, *sysgen* II.1-41
- System Generation, System-configuration File II.1-41
- System Hang V.4-2
- System Initialization V.3-9
- System manager, defined I.4-10
- System Memory Configuration V.3-9
- System Overview II.1-1
- System Power Up V.3-4
- System Specific Start-up Information, */etc/rc.local* II.A-23
- System Status Display II.1-35
- System status display, defined I.4-10
- System Status Display, SCM Error Codes — Quick Reference Table V.6-15
- System Status Display, SCM Error Codes Defined V.6-17
- System upgrade, cabinet installation III.5-27
- System upgrade, discussed III.5-1
- System upgrade, packing the C1 cabinet III.9-1
- System upgrade, removing the C1 III.5-2
- System-configuration File, Description II.1-41

T

- Table of contents, master, overview I.2-1
- TAC: reporting problems II.xviii, IV.xi, V.xiv, VI.xiii
- TAC, reporting problems to II.C-1, III.B-1, IV.B-1, V.E-1, VI.B-1
- Tape IV.2-18
- Tape, cipher cartridge IV.2-15
- Tape cleaner block, tape drives IV.2-16
- Tape Device Capability Database, */etc/tapecap* II.A-29
- Tape drive, tape path IV.2-15
- Tape drives IV.2-15
- Tape drives, Beginning of Tape/End of Tape IV.2-16
- Tape drives, capstan velocity and ramps IV.2-18
- Tape drives, column vacuum sensors IV.2-18
- Tape drives, diagnostics, internal IV.2-22
- Tape drives, fans IV.2-20
- Tape drives, file protect mechanism IV.2-18
- Tape drives, file reel null/gain IV.2-18

Tape drives, head alignment IV.2-17
 Tape drives, indicators IV.2-20
 Tape drives, machine reel null/gain IV.2-18
 Tape drives, pneumatics IV.2-19
 Tape drives, pneumatics, drive belts IV.2-19
 Tape drives, pneumatics levels IV.2-19
 Tape drives, power supply voltages IV.2-21
 Tape drives, preliminary reels null IV.2-18
 Tape drives, read output amplitudes IV.2-18
 Tape drives, rewind operations IV.2-19
 Tape drives, skew IV.2-16
 Tape drives, supply hub IV.2-17
 Tape drives, tape cleaner block IV.2-16
 Tape drives, tape path IV.2-15
tapecap File II.A-29
 Target CPU (TCPU) Register II.2-43
 TBD, abbreviation for To Be Determined I.x, III.x
 Technical Assistance Center. *See* TAC
 Technical Assistance Center, telephone numbers for I.xiii, I.1-4, III.xii
 Technical assistance, obtaining I.xiii, I.1-4, III.xii
 Teletypes, Root Login, File */etc/secretty* II.A-26
termcap II.A-33
termcap(3X) II.A-1
 Terminal, cabling III.4-2
 Terminal Configuration File, */etc/gettytab* II.A-7
 Terminal Initialization File, */etc/tty* II.A-31
 Terminal Types Database, */etc/ttytype* II.A-33
 Test Categories, Diagnostic, CONVEX C200 Series V.5-2
 Test Tag VI.3-15
 Thermal safety precautions VI.2-2
 Thread II.1-4
 Thread Allocation Count II.2-15
 Thread Allocation Mask II.2-15
 Thread Concurrency II.2-35
 Thread Timer II.2-53
 Thread-Level Page Table Entry (PTET) II.2-5
 Time of Century Clock (TOC) II.2-51
 Time of Century Counter II.7-9, II.7-11
 Time of Century Counter Functional Diagram II.7-11
 Timers II.2-49
tip Utility II.A-24
 TOC Clock, 64-Bit, Illustrated II.2-51
 Trace Trap Class Codes, Table II.2-36
 Trace Trap Qualifiers, Table II.2-36
 Transaction Types II.6-23
 Trap II.2-38
 Trap Instruction Register Partitioning, Illustrated II.2-38
 Trap Instruction Registers II.2-15
trap #rm, #b Instruction II.2-38
 Traps II.3-9
 Traps and Interrupts II.3-12
 Trouble reports I.xiii, I.1-4, II.xviii, III.xii, IV.xi, V.xiv, VI.xiii
 Troubleshooting CONVEX UNIX Error Messages, Flowchart V.10-1
 Troubleshooting Design Problem V.5-9
 Troubleshooting: Diagnostic Tests Fail Intermittently V.5-7
 Troubleshooting: Diagnostic Tests Fail Repeatedly V.5-7
 Troubleshooting: Failed Hardware V.5-9
 Troubleshooting: Intermittent System Failures V.5-6
 Troubleshooting: Repeatable System Failure; All Diagnostic Tests Pass V.5-7
 Troubleshooting SPU UNIX Error Messages, Flowchart V.9-1
 Troubleshooting System Failures V.5-4
 Troubleshooting With Diagnostic Tests, Flowchart V.5-1
 Troubleshooting With Diagnostics V.5-6
 Troubleshooting Wrong Answer V.5-5
 Troubleshooting: Diagnostic Tests Do Not Fail V.5-6
tset Program II.A-33
 TTR Manipulation II.2-53
ttys File II.A-31
ttytype File II.A-33
 Turning Power On. *See* Power-up Procedures

 U

Unencacheable Pages II.2-6
 UNIX Command Interpreters II.1-37
 UNIX, CONVEX, Description II.1-36
 UNIX, CONVEX, Multi-user, Description of II.1-40
 UNIX Crash V.4-2
 UNIX, defined I.4-10
 UNIX, Operating System II.1-3
 UNIX Processes, Explained V.4-1
 UNIX-to-UNIX Communication Protocols, with *contact* II.C-1, III.B-1, IV.B-1, V.E-1, VI.B-1
 Unpacking III.3-3
 Unshared Memory II.2-4
 Unsigned Numeric Value Data Type II.1-2
 Update Tags II.3-21
 Upgrade, cabinet installation III.5-27
 Upgrade, packing the C1 cabinet III.9-1
 Upgrade, removing the C1 III.5-2
 Upgrade, software III.8-2
 Upper rear plenum VI.4-48
 Upper rear plenum, illustrated VI.4-50
 Upper rear plenum, installation VI.4-50
 Upper rear plenum, removal VI.4-49
 Users, Adding New, */etc/nurc* II.A-14
 Using the IPB VI.5-1
 Utilities II.1-31
 Utility outlets, ratings III.2-1
 Utility Subsystem II.1-31
 Utility Subsystem, Illustrated II.7-1
 Utility Subsystem, Overview II.7-1
 UUCP. *See* UNIX-to-UNIX Communication Protocols
uucp(1), man page II.C-1, III.B-1, IV.B-1, V.E-1, VI.B-1

 V

Valid bit, defined I.4-10
 Valid reference, defined I.4-10
 Validity Tags II.3-21
 VBCU, Features, Described II.6-31
 VBCU, in VIOP System II.1-24
 VBCU. *See* VMEbus control unit
 Vector Address Generator (SFU) II.3-26
 Vector, defined I.4-10
 Vector Edit Logic II.4-9
 Vector Edit Operations, Multiply Pipe II.B-9
 Vector Element/Scalar, Move II.B-4
 Vector Index, Store using II.B-3
 Vector Instruction Operation, Overview II.B-1
 Vector Length Register II.4-14
 Vector Merge Register II.4-22
 Vector Operations, New II.2-2
 Vector Processor II.4-3
 Vector Processor Clocks, Table II.4-23
 Vector Processor Control, Illustrated II.4-4
 Vector Processor Data Pathways, Illustrated II.4-3
 Vector Processor Interfaces II.4-3
 Vector Processor Subsystem II.1-16
 Vector Processor Subsystem Functional Block Diagram, Illustrated II.4-1
 Vector Register File Gate Arrays, Illustrated II.4-6
 Vector Register File, Input Staging II.4-12
 Vector Register File, Output Staging II.4-13
 Vector Register Files II.4-6
 Vector Register, Load II.B-1
 Vector Register, Store II.B-2
 Vector Registers II.1-2
 Vector Register/Vector Index, Load II.B-2
 Vector Result Operations, ALU Pipe II.B-6
 Vector Subsystem, Overview II.4-1
vers II.C-1, III.B-1, IV.B-1, V.E-1, VI.B-1
 V/ESDI. *See* VMEbus/Enhanced interface disk controllers
 VIOP, Features II.1-24, II.6-29
 VIOP, Features, Discussed II.6-29
 VIOP Functional Diagram II.6-29
 VIOP, Overview II.1-24
 VIOP. *See* VMEbus Input/Output Processor
 VIOP. *See* VMEbus, Input/Output Processor

Master Index

VIPER Product Manual, SCSI Models 2060S and 2150S

I.1-3
vipw Utility II.A-21
Virtual Address Space II.1-3
Virtual address space. *See* Logical address space
Virtual Memory Management II.2-4
Virtual Memory Mapping Restrictions II.2-46
Virtual memory. *See* Logical memory
VL, Load II.B-4
VM Bit Output Staging Controller II.4-22
VM, Load II.B-4
VM, Store II.B-5
VME, defined I.4-10
VME Subsystem Block Diagram II.6-28
VMEbus Arbitration II.6-32
VMEbus chassis IV.2-12
VMEbus, defined I.4-10
VMEbus, fans IV.2-12
VMEbus, filters IV.2-12
VMEbus Input/Output Processor, cabling III.4-5, III.5-26
VMEbus Input/Output Processor, diagnostics III.7-5
VMEbus, power supply voltages IV.2-13
Voltages, 1960 tape drive power supply IV.2-21
Voltages, 2920 tape drive power supply IV.2-21
Voltages, disk drive power supply IV.2-15
Voltages, multibus power supply IV.2-12
Voltages, printer power supply IV.2-23
Voltages, processor power supply IV.2-6
Voltages, processor power supply, adjusting IV.2-9
Voltages, processor power supply, checking IV.2-8
Voltages, tape drive power supply IV.2-21
Voltages, VMEbus power supply IV.2-13
VPC #700 data flow, Block Diagram V.7-39
VPC #701 data flow, Block Diagram V.7-40
VPC #702 data flow, Block Diagram V.7-41
VPC #703 data flow, Block Diagram V.7-42
VPC #704 data flow, Block Diagram V.7-43
VPC Hard Errors V.7-39
VPD #800 data flow, Block Diagram V.7-44
VPD #801 data flow, Block Diagram V.7-45
VPD #802 data flow, Block Diagram V.7-46
VPD #803/#804 data flow, Block Diagram V.7-47
VPD Hard Errors V.7-44
VRF Input Bits, Table II.4-8
V/SMD. *See* VMEbus/Storage module device

W

wfork Instruction II.2-26
which II.C-1, III.B-1, IV.B-1, V.E-1, VI.B-1
Win Queue II.5-18
Wire Lists V.D-1
Word II.1-2
Word, defined I.4-10
Word Resource Structure Format, Illustrated II.2-19
Word Resource Structure With Two Pushed Entries, Illustrated II.2-20
Write Address Register (IPP) II.3-15
Write, defined I.4-10
Writing the Icache II.3-10
Wrong Answer Error V.4-2
Wrong Answer, Troubleshooting V.5-5
Wrong Answer/Core Dump V.4-2

Chapter 4

Glossary

4.1 Overview

The following terms are defined as they are used at CONVEX. Standard acronyms are also included. Boldfaced terms within a definition are defined in separate entries.

4.2 Terms

AC power-controller

In CONVEX supercomputers, the AC power-controller is the device that regulates AC power from the cabinet circuit breaker to the computer's internal electronic and electromechanical components.

access mode

Any of the five processor access modes in which software executes. On the CONVEX system, processor access modes are (in order from most to least privileged and protected): **kernel** (mode 0), **executive** (mode 1), **supervisor** (mode 2), **agent** (mode 3), and **user** (mode 4). The operating system uses access modes to define **protection** levels for software executing in the context of a **process**.

A register

See **address register**.

accumulator

A hardware register containing the results of arithmetic and logical operations.

address

A user-assigned number used by the operating system to identify a storage location.

address register

A register containing the address of the instruction currently being executed. Abbreviated A register.

address scalar processor

One of four processor boards that function as the Address and Scalar Unit. Sends to and receives from memory the read and write data requests. Abbreviated ASP. *See also* **instruction processor unit**, **data cache unit**, **scalar function unit**.

address space

Address space, either physical or virtual, available to a process.

address translation fault (ATF)

An **exception** that results from a **page table entry** violation or a nonresident page.

address translation unit (ATU)

Translates logical addresses to physical addresses and stores them in a **cache**; thus, the ATU is an address cache that accelerates the generation of **physical addresses**.

addressing mode

How the effective address of an instruction **operand** is calculated using the general registers.

agent Processor access mode 3.

ALU See **arithmetic logic unit**

architecture

The physical structure of a computer's internal operations, including its registers, memory, instruction set, input/output structure, and so on.

argument pointer

An address register specifically dedicated to point to the **subroutine** argument portion of a program. This program portion can either be in the **stack** or in part of **logical memory** pre-allocated by the **compiler**.

arithmetic logic unit

A basic element of the **Central Processing Unit** (CPU) where arithmetic and logical operations are performed. Abbreviated ALU.

array An ordered structure of operands of the same data type. The structure of an array is defined as: length, rank (or dimension), stride, and data type.

ATF See **address translation fault**.

ASP See **address scalar processor**.

ATU See **address translation unit**.

b See **byte**.

backplane

The circuitry and mechanical elements used to connect the boards of a system. Also called **motherboard**.

base-level interrupt

An interrupt that occurs when the kernel stack is the process stack; thus, a base-level interrupt occurs when no other interrupts are pending or currently being processed.

bit A binary digit.

bit complement

Exchanging 0's and 1's in the binary representation of a number.

block To stop the flow of execution. Execution cannot begin until the block no longer exists. Also called a **hazard**.

boot The procedure by which a program is initiated the first time. Typically, a bootstrap is performed when power is first applied to the processor.

branch A class of **instructions**, specifically relative to the program counter, used to transfer control of a program.

breakpoint

An instruction that aids in the debugging of a program. In particular, a breakpoint is a specific location in a program where one would desire to determine the various values of programmer-defined variables.

byte The number of contiguous bits starting on an addressable byte boundary. In CONVEX machines, a byte is 8 **bits**. Abbreviated **b**.

- C** The systems programming language of the UNIX operating system.
- C shell** The standard shell provided with Berkeley standard versions of UNIX.
- cache memory**
A small, high-speed buffer memory used in modern computer systems to hold temporarily those portion of the contents of the main memory that are, or believed to be, currently in use. CONVEX computers contain many separate caches, including **logical caches**, **physical caches**, and **instruction caches**.
- cache purge**
The act of invalidating or removing entries in a cache memory.
- central processing unit**
The Central Processing Unit (CPU) is that portion of a CONVEX computer that recognizes and executes the instruction set.
- chaining**
Chaining is the ability to overlap vector operations in the CPU. For instance, in the case of a **vector** load followed by a vector add, the add may be started as soon as the first operands are available, rather than waiting for the **load** to complete.
- chassis** The physical box where the computer is housed.
- compiler**
A software tool used to compile the source code of a high-level language, such as FORTRAN, into object code.
- CONVEX UNIX**
The CONVEX version of the UNIX operating system.
- CPU** *See* **central processing unit**.
- d** *See* **double**.
- data cache unit**
One of four processor boards that function as the Address and Scalar Unit. Contains part of the data cache datapath, all of the data cache control, and outgoing memory interface control logic. Abbreviated DCU. *See also* **address scalar processor**, **instruction processor unit**, **scalar function unit**.
- data type**
The way in which bits are grouped and interpreted. For processor instructions, the data type identifies the size of the operand and the significance of the bits in the operand.
- DCU** *See* **data cache unit**.
- destination**
The register or memory location that receives the result of the operation.
- displacement**
A derived 32-bit value used to indicate the distance in bytes between the referenced data and some base value. This base value can either be 0 or the contents of an address register. Note that 16-bit displacement values are sign extended to 32 bits.
- DMA** *See* **direct memory access**.
- DMAC** *See* **direct memory access controller**.
- EBUS** There are five ports on the memory system. These are referred to as ports A, B, C, D, and E. Ports A-D feed processors A-D; port E feeds the I/O system. Thus, EBUS is the bus to port E of the memory system.

electrostatic discharge

The release of static electricity from a charged object to a grounded object.

EMI Electromagnetic interference.

ESD *See electrostatic discharge.*

exception

A hardware-detected event that disrupts the running of a program, process, or system.
See also fault.

executive mode

Processor access mode 1.

expansion cabinet

A secondary cabinet designed to house peripheral computer equipment, e.g., tape drives, disk drives, controllers, etc. *See also processor cabinet.*

fault An exception that, while halting the instruction, leaves the **registers** and memory in a consistent state. The instruction can often resume its course when the cause of the fault is corrected.

FIFO Abbreviation for first-in, first-out. *See queue.*

firmware

Computer programs that are embodied in a physical device that can form part of a machine. Also, software that resides in **read-only memory**.

first-in, first-out

See queue.

flag A 1-bit operand that is generally used to indicate the results of an operation. The results are in the form true or false.

floating point

A numerical representation. A floating point operand has a sign (positive or negative) port, an exponent port, and a fraction port. The **fraction** is a fractional representation. The exponent is the value used to produce a power of two scale factor (or portion) that is subsequently used to multiply the fractions to produce an unsigned value. *See also fraction; guard bit.*

forced faulting mode

A mode of operation where the **CPU** diagnostics cause simulated **pagefaults** to occur. In forced faults mode, a bit is set in hardware so that each time data it is accessed in main memory, the entire context of the processor is saved off and then restored. This process thoroughly exercises the buses that are used to capture and restore the context of the machine as well as the entire memory system.

FORTRAN

A high-level software language used mainly for scientific applications.

fraction

A part of a **floating point** number. The fraction is the unsigned fractional part that denotes the magnitude of the operand.

frame *See page frame; stack frame*

fsck utility

A file systems check program used for maintenance and repair of data stored on disk.

function unit

A part of CPU that performs a set of operations on quantities stored in **registers**.

gate array

A structure that is used by the **ring** protection mechanism to define the entry points from a lower privileged ring to a higher privileged ring.

gather Loading a vector register using another vector of indices instruction. See the *ldvi* instruction.

guard bit

A bit to the right (**least significant bit**) of a floating point fraction. The guard bit is used in intermediate calculations using floating point operands. *See also* **round bit**.

h Abbreviation for halfword. *See* **halfword**.

halfword

Abbreviated **h**. Two bytes (16 bits). *See also* **longword**; **word**.

hazard A block in the flow of execution that cannot be passed until the hazard no longer exists. Also called **block**.

Icache *See* **instruction cache**.

immediates

Operands that are contained within the instruction stream.

indexing

The process of adding a **displacement** to the contents of an address register.

indirection

The process of obtaining the address of an operand by first referencing a word contained within memory.

Input/Output Processor

Abbreviated IOP. Channel Control Unit (CCU) used for I/O processing. Currently, there are two types of IOPs, one for the Multibus (MIOP) and one for the VMEbus (VIOP).

instruction

Used by the programmer to direct operations on the system's register set and memory.

instruction cache

The Instruction Cache (Icache) contains the most recently accessed instructions. The Icache accelerates the decoding of instructions to permit the simultaneous decoding on one instruction with the execution of another instruction.

instruction processor unit

Abbreviated IPP. One of four processor boards that function as the Address and Scalar Unit. *See also* **address scalar processor**, **data cache unit**, **scalar function unit**.

interrupt

An occurrence, other than an **exception**, that changes the normal flow of instruction execution. An interruption originates from hardware, such as an I/O device. *See also* **maskable interrupt**.

interval timer

A privileged register. The interval timer is used to generate an **interrupt** based on the passage of time.

IOP *See* **Input/Output Processor**.

IPP *See* **Instruction Processor Unit**.

jump Departure from normal one-step incrementing of the program counter.

kernel A part of the UNIX operating system that resides in ring0. The kernel typically manages process creation and deletion, scheduling, and other high-level, system-wide features.

keyswitch

On CONVEX supercomputers, a four-way electrical keyswitch that controls power-up and machine state.

l *See* **longword**.

load An instruction that moves data from memory to a register.

logical address

Logical address space is that **address space** seen by the application programmer.

logical cache

A cache that is accessed with **logical addresses** for fast retrieval of data. It resides in the **CPU**.

logical memory

That memory seen by the programmer. The logical memory of a CONVEX computer is 4 Gigabytes. Also called **virtual memory**. *See also* **page**.

longword

Abbreviated **l**. Eight bytes (64 bits), the largest integer data type directly supported by hardware in the CONVEX C120. *See also* **halfword**; **word**.

machine exceptions

Include fatal errors in the system that cannot be handled by the operating system. *See also* **exception**.

main memory

See **physical memory**.

maskable interrupt

An interrupt that the operating system does not wish not to respond to at this time.

MBCU *See* **multibus control unit**.

Mbyte *See* **megabyte**.

megabyte

1 million bytes, abbreviated **Mbyte**.

memory management

The hardware and software features that control page mapping and **protection**.

microcode

A control program that resides within the **CPU**. Microcode also refers to the firmware that provides the necessary control to map assembly language instructions onto processor hardware.

Multibus

An industry standard I/O bus that interfaces to the CONVEX Multibus Control Unit which, in turn, interfaces with the CONVEX MIOP. *See also* **Input/Output Processor**.

Multibus control unit

The Multibus Control Unit (MBCU) is the connecting link between the MIOP and the Multibus.

Multibus controller

Any device controller designed to function within the Multibus protocol. Multibus controllers plug into the Multibus cardcage.

Multibus cardcage

In CONVEX terminology, a chassis that provides a mounting frame for the Multibus (backplane) and support slots for installing Multibus controllers that plug into the Multibus. This term is synonymous with **Multibus drawer** and **Multibus chassis**.

multi-user mode

In CONVEX UNIX, the **mode** of operation where the supercomputer is being run in a general timesharing environment with multiple users. This is the normal operating mode for CONVEX UNIX. *See also single-user mode.*

page A page is the unit of logical memory controlled by the memory management algorithms. In the CONVEX C120, a page is 4 K (4,096) contiguous bytes. *See also logical memory.*

pagefault

A pagefault occurs when a process requests data that is not currently in main memory. The machine first saves off the state of all controllers onto a context stack in main memory. The operating system will create a free page of **physical memory** to bring the data in from the disk. The appropriate **Page Table Entries** (PTEs) are set up so that the proper logical-to-physical translation occurs. The machine reads back from memory the state of the machine from the context stack, and restores the processor to the same state that it was in when it determined that the data it needed was nonresident. The CPU can then continue with normal operation of the process.

page frame

A page frame is the unit of physical (main) memory in which pages are placed. Referenced and modified bits associated with each page frame aid in **memory management**.

page table entry

A Page Table Entry (PTE) is an entry in a page table. A PTE is a word that contains various **flags** and fields that are used in translation of logical-to-physical addresses. Address translation uses two levels of page table **indexing**. The first-level page table is referenced using bits <28> through <22> of a logical address. This is called the *Index.1* field. The second-level page table is referenced using bits <21> through <12> of a logical address. This is called the *Index.2* field.

PBUS The PBUS is the I/O channel between main memory and the channel control units.

PCU *See physical cache unit.*

physical address

Hardware-identified address in physical (main) memory consisting of the **page frame** number and the number of a byte within the page.

physical cache

Provides rapid access to recently used **physical memory** data items.

physical memory

This is main memory.

PIA See **peripheral bus interface adapter**.

pipeline

An overlapping operating cycle function that is used to increase the speed of computers. Pipelining provides a means by which multiple operations occur concurrently by beginning one instruction sequence before another has completed.

porting

Moving software from one type of machine to another.

process A process is the fundamental unit of a program that is managed by the **job scheduler**.

process exception

Belongs to the currently running process and may be handled with an **exception handler** in that process. The exception handler is in the current **ring** of execution.

processor cabinet

A cabinet designed to hold one or more **Central Processing Unit(s)** (CPUs).

processor status word

A Processor Status Word is a word that contains control **flags** used to control and indicate the states of various computations and sequences within the processor.

prompt

A character or character string sent from a computer system to a terminal to indicate to the user that the system is ready to accept input. Typical CONVEX prompts are (fp)>, #, %, :, and (spu)>.

protection

A mechanism provided by hardware and software that ensures that one user is protected from another user or to ensure that a user does not perform an unsafe computation.

PSW See **processor status word**.

PTE See **page table entry**.

queue A data structure in which entries are made at one end and deletions at the other. Often referred to as first-in, first-out (FIFO).

read A memory operation in which the contents of a memory location are accessed and passed to another part of the machine.

register

A hardware entity used to contain addresses, operands, and status.

reset The process of establishing a known state in a machine register.

rings A ring is the unit of logical memory used for **protection** purposes. There are five rings in CONVEX machines: four for system level usage and one for users. Each system ring (Ring0-Ring3) corresponds to one segment of logical memory, while the user ring (Ring4) contains four segments. User rings are Ring4-Ring7, collectively called Ring4.

root directory

The base directory in UNIX from which all other directories stem, directly or indirectly.

runtime

A software module that is referenced as a procedure. A runtime represents a required function that is not directly supported by the hardware, but is required by the software.

scalar function unit

Abbreviated SFU. One of four processor boards that function as the Address and Scalar Unit. Contains part of the data cache datapath and memory interface logic which handles handshakes to the memory system for the returning read data. *See also* **address scalar processor, data cache unit, instruction processor unit.**

SCM *See* **system control module.**

SCSI *See* **small computer system interface.**

SDR *See* **segment descriptor register.**

segment

The basic partition of the logical memory space, equal to 512 Mbytes.

segment descriptor register

Abbreviated SDR. Each segment of **virtual memory** has an SDR associated with it. Each SDR contains information pertinent to the access and mapping of virtual addresses.

segmented ALU

A logic design technique that permits multiple arithmetic operations of the same type to be **pipelined.**

SFU *See* **scalar function unit.**

shift A class of **instructions** used to shift the contents of a register right or left.

single-user mode

In CONVEX UNIX, the mode of operation where the supercomputer is being controlled by a single system manager or operator. This mode is used primarily for maintenance and system administrative functions. *See also* **multi-user mode.**

SMB *See* **system monitor board.**

soft front panel

EPROM-based software that controls certain **booting**, internal testing, and communications functions in CONVEX supercomputers.

software device driver

A CONVEX-supplied or user-written program that controls the operation of attached I/O peripheral devices.

SPU tape cartridge

The magnetic tape cartridge containing the SPU programs, files, and utilities.

SPU tape drive

The tape drive containing the SPU data.

SPU UNIX

The CONVEX-developed, UNIX-based software used to direct certain supervisory functions on CONVEX supercomputers.

stack A data structure in which the last item entered is the first to be removed. Also referred to as last-in, first-out (LIFO). In particular, stacks are used by the *call* and *return* instructions.

superuser

The UNIX term for the **system manager.**

system console

The CRT or printer/terminal that serves as a communication device between the **system manager** and CONVEX supercomputers.

system control module

The System Control Module (SCM) is an electronic safety mechanism that monitors hardware and environmental conditions on CONVEX C210 and C220 supercomputers. When an error condition is detected, the SCM transmits a hexadecimal status code to the system status display on the processor cabinet front panel.

system exceptions

Cannot be handled by the current process. They require intervention by the kernel executing in ring0. *See also exception.*

system manager

The person(s) responsible for the management and operation of a CONVEX supercomputer.

system status display

A two-digit LED display located on the front panel of CONVEX C210 and C220 supercomputers. It is used to display hexadecimal status codes transmitted by the SCM.

UNIX An operating system developed by AT&T Laboratories.

valid bit

Used for the control of **caches**. The valid bit is used to determine if a cache entry contains an entry that can be used.

valid reference

A valid reference meets two requirements: first, the **PTE** must be valid (bit $\langle 31 \rangle = 1$), and second, the type of access being made (read, write, or execute) must be allowed by the appropriate **protection** bits (bits $\langle 3..1 \rangle$ of the PTE).

VBCU *See VMEbus control unit.*

vector An **array** with one dimension.

virtual address space

See logical address space.

virtual memory

See logical memory.

VME Abbreviation for Versa Module European.

VMEbus

A popular 16-/32-bit I/O bus.

word Four bytes (32 bits), the fundamental width of items in the CONVEX family of computers. *See also halfword; longword.*

write A memory operation in which a memory location is updated with new data.

Index

A

A register. *See* Address register
AC power-controller, defined I.4-1
Access mode, defined I.4-1
Accumulator, defined I.4-1
Address, defined I.4-1
Address register, defined I.4-1
Address scalar processor, defined I.4-1
Address space, defined I.4-1
Address translation fault, defined I.4-1
Address translation unit, defined I.4-1
Addressing mode, defined I.4-2
Agent, defined I.4-2
ALU. *See* Arithmetic logic unit
Architecture, defined I.4-2
Argument pointer, defined I.4-2
Arithmetic logic unit, defined I.4-2
Arrays, defined I.4-2
ASP. *See* Address scalar processor
Associated documentation, listed I.1-3
Associated documentation, ordering I.1-3
ATF. *See* Address translation fault
ATU. *See* Address translation unit

B

b. *See* Byte
Backplane, defined I.4-2
Bit complement, defined I.4-2
Bit, defined I.4-2
Block, defined I.4-2
Boot, defined I.4-2
Branch, defined I.4-2
Breakpoint, defined I.4-2
Byte, defined I.4-2

C

C, defined I.4-3
C shell, defined I.4-3
C130, C210, C220 System Diagnostics, Release Notice
I.1-3
Cache, defined I.4-3
Cache purge, defined I.4-3
Cache. *See also* Instruction cache; Logical cache; Physical cache
Central processing unit, defined I.4-3
Chaining, defined I.4-3
Chassis, defined I.4-3
Compiler, defined I.4-3
CONVEX Architecture Reference I.1-3
CONVEX Computer Site Preparation Guide (C200 Series)
I.1-3
*CONVEX Diagnostic Database (C130, C210, C220),
Release Notice* I.1-3
CONVEX Diagnostic Documentation (C200 Series) I.1-3
CONVEX HIA User's Guide I.1-3
CONVEX Processor Operation Guide I.1-3
CONVEX Removable Disk System Operation Guide I.1-3
CONVEX System Manager's Guide I.1-3
CONVEX UNIX, defined I.4-3
CONVEX UNIX, Release Notice I.1-3
CONVEX VIOP/VBCU Service Guide I.1-3
CPU. *See* Central processing unit
Customer support, telephone numbers for I.1-4

D

d. *See* double
Data cache unit, defined
Data type, defined I.4-3
DCU. *See* Data cache unit
Destination, defined I.4-3
Displacement, defined I.4-3
DMA. *See* Direct memory access

Document numbers, format, in preface I.1-3
Documents, ordering, how to I.1-3

E

EBUS, defined I.4-3
Electrostatic discharge, defined I.4-4
EMI. *See* Electromagnetic interference
ESD. *See* Electrostatic discharge
Europe, technical assistance, how to obtain I.1-4
Exception, defined I.4-4
Executive mode, defined I.4-4
Expansion cabinet, defined I.4-4

F

Fault, defined I.4-4
FIFO. *See* Queue
Firmware, defined I.4-4
First-in, first-out. *See* Queue
Flag, defined I.4-4
Floating point, defined I.4-4
Forced faulting mode, defined I.4-4
FORTRAN, defined I.4-4
Fraction, defined I.4-4
Frame. *See* Page frame; Stack frame
fsck utility, defined I.4-4
*FUJITSU M2351A/AF Mini Disk Drive, Customer
Engineering Manual* I.1-3
Function unit, defined I.4-5

G

Gate array, defined I.4-5
Gather, defined I.4-5
Guard bit, defined I.4-5

H

h. *See* Halfword
Halfword, defined I.4-5

I

Icache. *See* Instruction cache
Immediates, defined I.4-5
Index, master, overview I.3-1
Indexing, register, defined I.4-5
Indirection, defined I.4-5
Input/output processor, defined I.4-5
Installation Procedure, CONVEX UNIX and Utilities I.1-3
Instruction cache, defined I.4-5
Instruction, defined I.4-5
Instruction processor unit, defined
Interrupt, defined I.4-5
Interrupts, base-level, defined I.4-2
Interval timer, defined I.4-5
IOP. *See* Input/output processor
IPP. *See* Instruction processor unit

J

Jump, defined I.4-6

K

Kernel, defined I.4-6
Keyswitch, defined I.4-6

Index

L

l. *See* Longword
Load, defined I.4-6
Logical address, defined I.4-6
Logical cache, defined I.4-6
Logical memory, defined I.4-6
Longword, defined I.4-6

M

Machine exceptions, defined I.4-6
Main memory. *See* Physical memory
Maintenance documentation, overview I.1-1
Maskable interrupt, defined I.4-6
Master index. *See* Index, master
Master table of contents. *See* Table of contents, master
MBCU. *See* Multibus control unit
Mbyte. *See* Megabyte
Megabyte, defined I.4-6
Memory management, defined I.4-6
Microcode, defined I.4-6
Multibus cardcage, defined I.4-7
Multibus control unit, defined I.4-7
Multibus controller, defined I.4-7
Multibus, defined I.4-6
Multi-user mode, defined I.4-7

O

Order numbers, format, in preface I.1-3
Ordering documentation, how to I.1-3
Overview, maintenance documentation I.1-1
Overview, master index I.3-1
Overview, master table of contents I.2-1

P

Page, defined I.4-7
Page frame, defined I.4-7
Page table entry, defined I.4-7
Pagefault, defined I.4-7
Part numbers. *See* Document numbers
PBUS, defined I.4-7
PCU. *See* Physical cache unit
Physical address, defined I.4-7
Physical cache, defined I.4-7
Physical memory, defined I.4-7
PIA. *See* Peripheral bus interface adapter
Pipeline, defined I.4-8
Porting, defined I.4-8
Printronic P6000 Maintenance Manual I.1-3
Process, defined I.4-8
Process exception, defined I.4-8
Processor cabinet, defined I.4-8
Processor status word, defined I.4-8
Programmable interrupt timer, defined I.4-8
Protection, defined I.4-8
PSW. *See* Processor status word
PTE. *See* Page table entry

Q

Queue, defined I.4-8

R

Read, defined I.4-8
Register, defined I.4-8
Reporting problems I.1-4
Reset, defined I.4-8
Revision sheet 3

Rings, defined I.4-8
Root directory, defined I.4-8
Runtime, defined I.4-8

S

Scalar function unit, defined I.4-9
SCM. *See* System control module
SCSI. *See* Small computer system interface
SDR. *See* Segment descriptor register
See Direct memory access controller, defined
Segment, defined I.4-9
Segment descriptor register, defined I.4-9
Segmented ALU, defined I.4-9
SFU. *See* Scalar function unit
Shift, defined I.4-9
Single(s), defined I.4-9
SMB. *See* System monitor board
Soft front panel, defined I.4-9
Software device driver, defined I.4-9
SPU tape cartridge, defined I.4-9
SPU tape drive, defined I.4-9
SPU UNIX, defined I.4-9
SPU UNIX, Release Notice I.1-3
Stack, defined I.4-9
STC 1960 Series Tape Drive I.1-3
STC 2920 Tape Subsystem Maintenance Manual I.1-3
Supervisor, defined I.4-9
System console, defined I.4-10
System control module, defined I.4-10
System exceptions, defined I.4-10
System manager, defined I.4-10
System status display, defined I.4-10

T

Table of contents, master, overview I.2-1
Technical Assistance Center, telephone numbers for I.1-4
Technical assistance, obtaining I.1-4
Trouble reports I.1-4

U

UNIX, defined I.4-10

V

Valid bit, defined I.4-10
Valid reference, defined I.4-10
VBCU. *See* VMEbus control unit
Vector, defined I.4-10
VIPER Product Manual, SCSI Models 2060S and 2150S
I.1-3
Virtual address space. *See* Logical address space
Virtual memory. *See* Logical memory
VME, defined I.4-10
VMEbus, defined I.4-10

W

Word, defined I.4-10
Write, defined I.4-10

(Fold Here First)



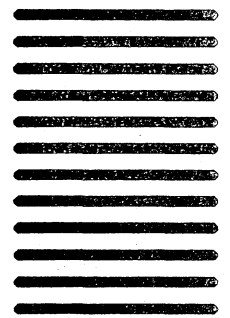
NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 1046 RICHARDSON, TEXAS

POSTAGE WILL BE PAID BY ADDRESSEE

CUSTOMER SERVICE
CONVEX Computer Corp.
P.O. Box 833851
Richardson, TX 75083-3851



(Fold Here Second)

(Tape or Staple)