Ronald Gphof

CONVEX Maintenance Documentation Overview (C201, C202, C210, C220)

Document No. 081-000003-201

First Edition, Rev. 1
February 1989

CONVEX Computer Corporation
Richardson, Texas USA

CONVEX Maintenance Documentation Overview
(C201, C202, C210, C220)
Order No. DHW-100
First Edition, Rev. 1

Printed in the United States of America

Revision Sheet

CONVEX Maintenance Documentation Overview
(C201, C202, C210, C220)

Edition	Document No.	Date	Description
First	081-000003-200	September 1988	Describes the five manuals comprising the *CONVEX Maintenance Documentation* kit. Provides a master table of contents, index, and glossary to all manuals.
First, Rev. 1	081-000003-201	February 1989	Minor corrections made to Volumes I–IV and VI; corrections and major additions made to Volume V.

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Table of Contents

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Chapter 1
Introduction

1.1 Overview

CONVEX Maintenance Documentation (C201, C202, C210, C220) contains five separate volumes of maintenance materials plus this overview manual. This manual introduces the structure of the *CONVEX Maintenance Documentation (C201, C202, C210, C220).* It also includes a master table of contents, a master index, and a master glossary to all six volumes.

The *CONVEX Maintenance Documentation (C201, C202, C210, C220)* is a reference tool for CONVEX personnel who maintain CONVEX equipment and CONVEX customers who do their own maintenance.

1.2 Scope

The *CONVEX Maintenance Documentation* applies to the CONVEX C201, C202, C210, and C220 supercomputers.

1.3 Documents Included

This documentation kit includes the following six maintenance manuals:

- Volume I, *CONVEX Maintenance Documentation Overview (C201, C202, C210, C220)*—Use this manual to obtain a general overview of the documentation as well as find the master table of contents, master index, and master glossary to all documentation.
- Volume II, *CONVEX Theory of Operation (C201, C202, C210, C220)*—This document contains a broad system-level introduction and theory to the level necessary to support maintenance.
- Volume III, *CONVEX Installation Guide (C201, C202, C210, C220)*—This volume provides procedures for installing a system at a new site and for upgrading a system at an existing site.
- Volume IV, *CONVEX General Maintenance Guide (C201, C202, C210, C220)*—This document provides a preventive maintenance schedule and procedures for maintaining a system on a monthly and quarterly basis.
- Volume V, *CONVEX Troubleshooting Guide (C201, C202, C210, C220)*—This document provides indicator and error message information, troubleshooting procedures and flow charts, and a troubleshooting philosophy and methodology discussion.
- Volume VI, *CONVEX Removal/Replacement and IPB Guide (C201, C202, C210, C220)*—This guide provides the Field Engineer (FE) with the information required to remove, order, and install components in the computer.

1.4 Dependencies

All volumes in this kit are designed to be used together to eliminate excessive repetition of technical data between manuals and to simplify the revision process. The master table of contents, master index, and master glossary are comprehensive reference tools that make using the kit easier.

1.5 Master Table of Contents

A master table of contents, in Chapter 2, contains an exact copy of the table of contents of each volume.

1.6 Master Index

The master index, in Chapter 3, makes finding a particular subject easier across all volumes. The index contains symbol and numeric sections as well as the usual alphabetical section. Alphabetization is in the following order:

1. symbols
2. numerals
3. letters from A to Z

Each section is preceded by a boldfaced title. Preceding each page number (which is the chapter number followed by a dash then the page number of that chapter) is a Roman numeral that indicates the volume referenced. A period is placed between the volume number and the chapter-page number. The following is an example index entry:

System Exerciser, *sysex* III.8-2, IV.3-5

The above entry indicates that references to the system exerciser program appear in volume III (*CONVEX Installation Guide (C201, C202, C210, C220)*) on page 2 of Chapter 8, and in volume IV (*CONVEX General Maintenance Guide (C201, C202, C210, C220)*) on page 5 of Chapter 3.

See cross-references guide the reader to preferred spellings and entry wording. *See also* cross-references point the way to related subjects.

1.7 Master Glossary

The master glossary, in Chapter 4, is a list of CONVEX-preferred technical nomenclature and terminology, including standard abbreviations.

1.8 Associated Documentation

The following is a partial list of other manuals or books that may provide more detailed information on the topics presented in this manual:

- *C130, C210, C220 System Diagnostics, Release Notice*
- *CONVEX Architecture Reference*, Product No. DHW-005
- *CONVEX Computer Site Preparation Guide (C200 Series)*, Order No. DHW-009
- *CONVEX Diagnostic Database (C130, C210, C220), Release Notice*
- *CONVEX Diagnostic Documentation (C200 Series)*, Product No. DHW-080
- *CONVEX HIA User's Guide*, Product No. DHW-035
- *CONVEX Processor Operation Guide (C100 Series, C200 Series)*, Order No. DHW-015
- *CONVEX Removable Disk System Operation Guide*, Order No. DHW-043
- *CONVEX System Manager's Guide*, Product No. DSW-004
- *CONVEX UNIX, Release Notice*
- *CONVEX VIOP/VBCU Service Guide*, Product No. DHW-051
- *FUJITSU M2351A/AF Mini Disk Drive, Customer Engineering Manual*
- *Installation Procedure, CONVEX UNIX and Utilities*
- *Printronix P6000 Maintenance Manual*, Document No. 900-000328-001
- *SPU UNIX, Release Notice*
- *STC 1960 Series Tape Drive*, Document No. 900-000253-001
- *STC 2920 Tape Subsystem Maintenance Manual*, Document No. 900-000252-001
- *VIPER Product Manual, SCSI Models 2060S and 2150S*, Document No. 900-000321-001

1.8.1 Ordering Documentation

To obtain the most current version of this or any other CONVEX document, use the order number. If the product number is not known, order by the exact title. In some situations the most current version is not desired. To receive a specific version of a manual, use the CONVEX document, or part, number, which can be obtained by contacting the local CONVEX office or by calling the Technical Assistance Center.

The product number for this manual is DHW-100.
The document number for this manual is 081-000003-201.

CONVEX documents can be ordered by mail by sending a request to:

CONVEX Computer Corporation
Customer Service
PO Box 833851
Richardson TX 75083-3851 USA

1.8.2 Technical Assistance

Hardware and software support can be obtained through the CONVEX Technical Assistance Center (TAC). The TAC can be reached in Texas by calling (214) 952-0379, or by calling 1(800) 952-0379 from other locations in the continental United States. Customers outside the United States should contact their local CONVEX office.

Electronic Mail

The Hardware Documentation Group has an email address for documentation comments. Use this service to give us a quick response mechanism if you have special documentation questions that you would like addressed immediately. If you have a technical question, you should still contact the Technical Assistance Center, as described previously. To use email response service, just send mail addressed to:

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cnvxhwdoc@convex.COM
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We will read your comments and give you a personal reply.

What to Include in an Email Message

When you use the electronic mail service, please provide the following information:

- The reader's name and company name
- A return email address in INTERNET notation or UUCP (bang) notation
- The manual that is being critiqued
- The chapter and page number in question
- The comment

Reader's Forum

If you wish to mail your comments to us, please use the form at the end of this manual and list the document page number with your questions and comments. Thank you.

Acknowledgments

I would like to thank the following people for their contributions to the volumes of this document kit:

- Technical contributors: Rich Adkisson, Tony Brewer, Art Clark, Mary Cooley, Brad Culter, Gary Gostin, Carl Jackson, Jeff Jones, Tony Jones, Art Kimmel, Brian Konigsburg, Kevin Lowderman, Alan Peterson, Marc Quattromani, John Rachels, and Craig Reed
- Review team members: Art Clark, Don Davis, Ron Engelking, Steve Fieler, Art Kimmel, and Rick Miller
- Hardware Documentation staff: Larry Bonura, Art Fischman, and Jimmie Holman
- Contributing writers: Bruce Evans, Barbara Morris, and Randy Stiles

Without the efforts of all the aforementioned, this document would not have been possible.

Leigh Ellert, Lead Writer
CONVEX Hardware Documentation

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Chapter 2
Master Table of Contents

2.1 Overview

This chapter contains the master table of contents, which gives a comprehensive outline of the six volumes in this kit.

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Chapter 3
Master Index

3.1 Overview

This chapter contains the master index to the six volumes that comprise the *CONVEX Maintenance Documentation* kit.

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Chapter 4
Glossary

4.1 Overview

The following terms are defined as they are used at CONVEX. Standard acronyms are also included. Boldfaced terms within a definition are defined in separate entries.

4.2 Terms

AC power-controller
In CONVEX supercomputers, the AC power-controller is the device that regulates AC power from the cabinet circuit breaker to the computer's internal electronic and electromechanical components.

access mode
Any of the five processor access modes in which software executes. On the CONVEX system, processor access modes are (in order from most to least privileged and protected): **kernel** (mode 0), **executive** (mode 1), **supervisor** (mode 2), **agent** (mode 3), and **user** (mode 4). The operating system uses access modes to define **protection** levels for software executing in the context of a **process**.

A register
See **address register**.

accumulator
A hardware register containing the results of arithmetic and logical operations.

address
A user-assigned number used by the operating system to identify a storage location.

address register
A register containing the address of the instruction currently being executed. Abbreviated A register.

address scalar processor
One of four processor boards that function as the Address and Scalar Unit. Sends to and receives from memory the read and write data requests. Abbreviated ASP. *See also* **instruction processor unit**, **data cache unit**, **scalar function unit**.

address space
Address space, either physical or virtual, available to a process.

address translation fault (ATF)
An **exception** that results from a **page table entry** violation or a nonresident page.

address translation unit (ATU)
Translates logical addresses to physical addresses and stores them in a **cache**; thus, the ATU is an address cache that accelerates the generation of **physical addresses**.

addressing mode
How the effective address of an instruction **operand** is calculated using the general registers.

agent Processor access mode 3.

ALU *See* **arithmetic logic unit**

architecture
The physical structure of a computer's internal operations, including its registers, memory, instruction set, input/output structure, and so on.

argument pointer
An address register specifically dedicated to point to the **subroutine** argument portion of a program. This program portion can either be in the **stack** or in part of **logical memory** pre-allocated by the **compiler**.

arithmetic logic unit
A basic element of the **Central Processing Unit** (CPU) where arithmetic and logical operations are performed. Abbreviated ALU.

array An ordered structure of operands of the same data type. The structure of an array is defined as: length, rank (or dimension), stride, and data type.

ATF *See* **address translation fault.**

ASP *See* **address scalar processor.**

ATU *See* **address translation unit.**

b *See* **byte.**

backplane
The circuitry and mechanical elements used to connect the boards of a system. Also called **motherboard.**

base-level interrupt
An interrupt that occurs when the kernel stack is the process stack; thus, a base-level interrupt occurs when no other interrupts are pending or currently being processed.

bit A binary digit.

bit complement
Exchanging 0's and 1's in the binary representation of a number.

block To stop the flow of execution. Execution cannot begin until the block no longer exists. Also called a **hazard.**

boot The procedure by which a program is initiated the first time. Typically, a bootstrap is performed when power is first applied to the processor.

branch A class of **instructions**, specifically relative to the program counter, used to transfer control of a program.

breakpoint
An instruction that aids in the debugging of a program. In particular, a breakpoint is a specific location in a program where one would desire to determine the various values of programmer-defined variables.

byte The number of contiguous bits starting on an addressable byte boundary. In CONVEX machines, a byte is 8 **bits**. Abbreviated **b**.

C The systems programming language of the **UNIX** operating system.

C shell The standard shell provided with Berkeley standard versions of UNIX.

cache memory
A small, high-speed buffer memory used in modern computer systems to hold temporarily those portion of the contents of the main memory that are, or believed to be, currently in use. CONVEX computers contain many separate caches, including **logical caches**, **physical caches**, and **instruction caches**.

cache purge
The act of invalidating or removing entries in a cache memory.

central processing unit
The Central Processing Unit (CPU) is that portion of a CONVEX computer that recognizes and executes the instruction set.

chaining
Chaining is the ability to overlap vector operations in the CPU. For instance, in the case of a **vector** load followed by a vector add, the add may be started as soon as the first operands are available, rather than waiting for the **load** to complete.

chassis The physical box where the computer is housed.

compiler
A software tool used to compile the source code of a high-level language, such as FORTRAN, into object code.

CONVEX UNIX
The CONVEX version of the UNIX operating system.

CPU *See* **central processing unit.**

d *See* **double.**

data cache unit
One of four processor boards that function as the Address and Scalar Unit. Contains part of the data cache datapath, all of the data cache control, and outgoing memory interface control logic. Abbreviated DCU. *See also* **address scalar processor**, **instruction processor unit**, **scalar function unit.**

data type
The way in which bits are grouped and interpreted. For processor instructions, the data type identifies the size of the operand and the significance of the bits in the operand.

DCU *See* **data cache unit.**

destination
The register or memory location that receives the result of the operation.

displacement
A derived 32-bit value used to indicate the distance in bytes between the referenced data and some base value. This base value can either be 0 or the contents of an address register. Note that 16-bit displacement values are sign extended to 32 bits.

DMA *See* **direct memory access.**

DMAC *See* **direct memory access controller.**

EBUS There are five ports on the memory system. These are referred to as ports A, B, C, D, and E. Ports A–D feed processors A–D; port E feeds the I/O system. Thus, EBUS is the bus to port E of the memory system.

electrostatic discharge
The release of static electricity from a charged object to a grounded object.

EMI Electromagnetic interference.

ESD *See* **electrostatic discharge.**

exception
A hardware-detected event that disrupts the running of a program, process, or system. *See also* **fault.**

executive mode
Processor access mode 1.

expansion cabinet
A secondary cabinet designed to house peripheral computer equipment, e.g., tape drives, disk drives, controllers, etc. *See also* **processor cabinet.**

fault An exception that, while halting the instruction, leaves the **registers** and memory in a consistent state. The instruction can often resume its course when the cause of the fault is corrected.

FIFO Abbreviation for first-in, first-out. *See* **queue.**

firmware
Computer programs that are embodied in a physical device that can form part of a machine. Also, software that resides in **read-only memory**.

first-in, first-out
See **queue.**

flag A 1-bit operand that is generally used to indicate the results of an operation. The results are in the form true or false.

floating point
A numerical representation. A floating point operand has a sign (positive or negative) port, an exponent port, and a fraction port. The **fraction** is a fractional representation. The exponent is the value used to produce a power of two scale factor (or portion) that is subsequently used to multiply the fractions to produce an unsigned value. *See also* **fraction; guard bit.**

forced faulting mode
A mode of operation where the **CPU** diagnostics cause simulated **pagefaults** to occur. In forced faults mode, a bit is set in hardware so that each time data it is accessed in main memory, the entire context of the processor is saved off and then restored. This process thoroughly exercises the buses that are used to capture and restore the context of the machine as well as the entire memory system.

FORTRAN
A high-level software language used mainly for scientific applications.

fraction
A part of a **floating point** number. The fraction is the unsigned fractional part that denotes the magnitude of the operand.

frame *See* **page frame; stack frame**

***fsck* utility**
A file systems check program used for maintenance and repair of data stored on disk.

function unit
A part of **CPU** that performs a set of operations on quantities stored in **registers**.

gate array
A structure that is used by the **ring** protection mechanism to define the entry points from a lower privileged ring to a higher privileged ring.

gather Loading a vector register using another vector of indices instruction. See the *ldvi* instruction.

guard bit
A bit to the right (**least significant bit**) of a floating point fraction. The guard bit is used in intermediate calculations using floating point operands. *See also* **round bit**.

h Abbreviation for halfword. *See* **halfword**.

halfword
Abbreviated **h**. Two bytes (16 bits). *See also* **longword**; **word**.

hazard A block in the flow of execution that cannot be passed until the hazard no longer exists. Also called **block**.

Icache *See* **instruction cache**.

immediates
Operands that are contained within the instruction stream.

indexing
The process of adding a **displacement** to the contents of an address register.

indirection
The process of obtaining the address of an operand by first referencing a word contained within memory.

Input/Output Processor
Abbreviated IOP. Channel Control Unit (CCU) used for I/O processing. Currently, there are two types of IOPs, one for the Multibus (MIOP) and one for the VMEbus (VIOP).

instruction
Used by the programmer to direct operations on the system's register set and memory.

instruction cache
The Instruction Cache (Icache) contains the most recently accessed instructions. The Icache accelerates the decoding of instructions to permit the simultaneous decoding on one instruction with the execution of another instruction.

instruction processor unit
Abbreviated IPP. One of four processor boards that function as the Address and Scalar Unit. *See also* **address scalar processor**, **data cache unit**, **scalar function unit**.

interrupt
An occurrence, other than an **exception**, that changes the normal flow of instruction execution. An interruption originates from hardware, such as an I/O device. *See also* **maskable interrupt**.

interval timer
A privileged register. The interval timer is used to generate an **interrupt** based on the passage of time.

IOP *See* **Input/Output Processor.**

IPP *See* **Instruction Processor Unit.**

jump Departure from normal one-step incrementing of the program counter.

kernel A part of the UNIX operating system that resides in ring0. The kernel typically manages process creation and deletion, scheduling, and other high-level, system-wide features.

keyswitch
On CONVEX supercomputers, a four-way electrical keyswitch that controls power-up and machine state.

l *See* **longword.**

load An instruction that moves data from memory to a register.

logical address
Logical address space is that **address space** seen by the application programmer.

logical cache
A cache that is accessed with **logical addresses** for fast retrieval of data. It resides in the **CPU.**

logical memory
That memory seen by the programmer. The logical memory of a CONVEX computer is 4 Gigabytes. Also called **virtual memory.** *See also* **page.**

longword
Abbreviated l. Eight bytes (64 bits), the largest integer data type directly supported by hardware in the CONVEX C120. *See also* **halfword; word.**

machine exceptions
Include fatal errors in the system that cannot be handled by the operating system. *See also* **exception.**

main memory
See **physical memory.**

maskable interrupt
An interrupt that the operating system does not wish not to respond to at this time.

MBCU *See* **multibus control unit.**

Mbyte *See* **megabyte.**

megabyte
1 million bytes, abbreviated Mbyte.

memory management
The hardware and software features that control page mapping and **protection.**

microcode
A control program that resides within the CPU. Microcode also refers to the firmware that provides the necessary control to map assembly language instructions onto processor hardware.

Multibus
An industry standard I/O bus that interfaces to the CONVEX Multibus Control Unit which, in turn, interfaces with the CONVEX MIOP. *See also* **Input/Output Processor.**

Multibus control unit
The Multibus Control Unit (MBCU) is the connecting link between the **MIOP** and the **Multibus**.

Multibus controller
Any device controller designed to function within the Multibus protocol. Multibus controllers plug into the Multibus cardcage.

Multibus cardcage
In CONVEX terminology, a chassis that provides a mounting frame for the Multibus (backplane) and support slots for installing Multibus controllers that plug into the Multibus. This term is synonymous with **Multibus drawer** and **Multibus chassis**.

multi-user mode
In **CONVEX UNIX**, the **mode** of operation where the supercomputer is being run in a general timesharing environment with multiple users. This is the normal operating mode for CONVEX UNIX. *See also* **single-user mode**.

page A page is the unit of logical memory controlled by the memory management algorithms. In the CONVEX C120, a page is 4 K (4,096) contiguous bytes. *See also* **logical memory**.

pagefault
A pagefault occurs when a process requests data that is not currently in main memory. The machine first saves off the state of all controllers onto a context stack in main memory. The operating system will create a free page of **physical memory** to bring the data in from the disk. The appropriate **Page Table Entries** (PTEs) are set up so that the proper logical-to-physical translation occurs. The machine reads back from memory the state of the machine from the context stack, and restores the processor to the same state that it was in when it determined that the data it needed was nonresident. The CPU can then continue with normal operation of the process.

page frame
A page frame is the unit of physical (main) memory in which pages are placed. Referenced and modified bits associated with each page frame aid in **memory management.**

page table entry
A Page Table Entry (PTE) is an entry in a page table. A PTE is a word that contains various **flags** and fields that are used in translation of logical-to-physical addresses. Address translation uses two levels of page table **indexing**. The first-level page table is referenced using bits <28> through <22> of a logical address. This is called the *Index.1* field. The second-level page table is referenced using bits <21> through <12> of a logical address. This is called the *Index.2* field.

PBUS The PBUS is the I/O channel between main memory and the channel control units.

PCU *See* **physical cache unit**.

physical address
Hardware-identified address in physical (main) memory consisting of the **page frame** number and the number of a byte within the page.

physical cache
Provides rapid access to recently used **physical memory** data items.

physical memory
This is main memory.

PIA *See* **peripheral bus interface adapter.**

pipeline
An overlapping operating cycle function that is used to increase the speed of computers. Pipelining provides a means by which multiple operations occur concurrently by beginning one instruction sequence before another has completed.

porting
Moving software from one type of machine to another.

process A process is the fundamental unit of a program that is managed by the **job scheduler**.

process exception
Belongs to the currently running process and may be handled with an **exception** handler in that process. The exception handler is in the current **ring** of execution.

processor cabinet
A cabinet designed to hold one or more **Central Processing Unit(s)** (CPUs).

processor status word
A Processor Status Word is a word that contains control **flags** used to control and indicate the states of various computations and sequences within the processor.

prompt
A character or character string sent from a computer system to a terminal to indicate to the user that the system is ready to accept input. Typical CONVEX prompts are (fp)>, #, %, :, and (spu)>.

protection
A mechanism provided by hardware and software that ensures that one user is protected from another user or to ensure that a user does not perform an unsafe computation.

PSW *See* **processor status word.**

PTE *See* **page table entry.**

queue A data structure in which entries are made at one end and deletions at the other. Often referred to as first-in, first-out (FIFO).

read A memory operation in which the contents of a memory location are accessed and passed to another part of the machine.

register
A hardware entity used to contain addresses, operands, and status.

reset The process of establishing a known state in a machine register.

rings A ring is the unit of logical memory used for **protection** purposes. There are five rings in CONVEX machines: four for system level usage and one for users. Each system ring (Ring0-Ring3) corresponds to one segment of logical memory, while the user ring (Ring4) contains four segments. User rings are Ring4–Ring7, collectively called Ring4.

root directory
The base directory in UNIX from which all other directories stem, directly or indirectly.

runtime
A software module that is referenced as a procedure. A runtime represents a required function that is not directly supported by the hardware, but is required by the software.

scalar function unit
Abbreviated SFU. One of four processor boards that function as the Address and Scalar Unit. Contains part of the data cache datapath and memory interface logic which handles handshakes to the memory system for the returning read data. *See also* **address scalar processor, data cache unit, instruction processor unit.**

SCM *See* **system control module.**

SCSI *See* **small computer system interface.**

SDR *See* **segment descriptor register.**

segment
The basic partition of the logical memory space, equal to 512 Mbytes.

segment descriptor register
Abbreviated SDR. Each segment of **virtual memory** has an SDR associated with it. Each SDR contains information pertinent to the access and mapping of virtual addresses.

segmented ALU
A logic design technique that permits multiple arithmetic operations of the same type to be **pipelined.**

SFU *See* **scalar function unit.**

shift A class of **instructions** used to shift the contents of a register right or left.

single-user mode
In CONVEX UNIX, the mode of operation where the supercomputer is being controlled by a single system manager or operator. This mode is used primarily for maintenance and system administrative functions. *See also* **multi-user mode.**

SMB *See* **system monitor board.**

soft front panel
EPROM-based software that controls certain **booting**, internal testing, and communications functions in CONVEX supercomputers.

software device driver
A CONVEX-supplied or user-written program that controls the operation of attached I/O peripheral devices.

SPU tape cartridge
The magnetic tape cartridge containing the SPU programs, files, and utilities.

SPU tape drive
The tape drive containing the SPU data.

SPU UNIX
The CONVEX-developed, UNIX-based software used to direct certain supervisory functions on CONVEX supercomputers.

stack A data structure in which the last item entered is the first to be removed. Also referred to as last-in, first-out (LIFO). In particular, stacks are used by the *call* and *return* instructions.

superuser
The UNIX term for the **system manager.**

system console
The CRT or printer/terminal that serves as a communication device between the **system manager** and CONVEX supercomputers.

system control module
The System Control Module (SCM) is an electronic safety mechanism that monitors hardware and environmental conditions on CONVEX C210 and C220 supercomputers. When an error condition is detected, the SCM transmits a hexadecimal status code to the system status display on the processor cabinet front panel.

system exceptions
Cannot be handled by the current process. They require intervention by the **kernel** executing in ring0. *See also* **exception.**

system manager
The person(s) responsible for the management and operation of a CONVEX supercomputer.

system status display
A two-digit LED display located on the front panel of CONVEX C210 and C220 supercomputers. It is used to display hexadecimal status codes transmitted by the SCM.

UNIX An operating system developed by AT&T Laboratories.

valid bit
Used for the control of **caches.** The valid bit is used to determine if a cache entry contains an entry that can be used.

valid reference
A valid reference meets two requirements: first, the **PTE** must be valid (bit <31>=1), and second, the type of access being made (read, write, or execute) must be allowed by the appropriate **protection** bits (bits <3..1> of the PTE).

VBCU *See* **VMEbus control unit.**

vector An **array** with one dimension.

virtual address space
See **logical address space.**

virtual memory
See **logical memory.**

VME Abbreviation for Versa Module European.

VMEbus
A popular 16-/32-bit I/O bus.

word Four bytes (32 bits), the fundamental width of items in the CONVEX family of computers. *See also* **halfword**; **longword.**

write A memory operation in which a memory location is updated with new data.

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Reader's Forum

You are invited to submit comments about the clarity and service of this manual. Constructive critical comments are most welcome, and will help us continue in our efforts to generate quality customer documentation. Please list the document page number with your questions and comments.

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FOR ADDITIONAL INFORMATION OR DOCUMENTATION:

Location	Phone Number
In Texas	(214)952-0200
Other continental locations	1(800)952-0379
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Richardson TX 75083-3851 USA

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